DATA TRANSLATION

UM-24349-N

DT9862 Series User's Manual

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Radio and Television Interference

This equipment has been tested and found to comply with CISPR EN55022 Class A and EN61000-6-1 requirements and also with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Changes or modifications to this equipment not expressly approved by Data Translation could void your authority to operate the equipment under Part 15 of the FCC Rules.

Note: This product was verified to meet FCC requirements under test conditions that included use of shielded cables and connectors between system components. It is important that you use shielded cables and connectors to reduce the possibility of causing interference to radio, television, and other electronic devices.

Canadian Department of Communications Statement

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class A prescrites dans le Règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.

Table of Contents

About this Manual

The first part of this manual describes how to install and set up your DT9862 Series module and device driver, and verify that your module is working properly.

The second part of this manual describes the features of the DT9862 Series modules, the capabilities of the DT9862 Series Device Driver, and how to program the DT9862 Series modules using DT-Open Layers for .NET Class Library™ software. Troubleshooting information is also provided.

Notes: For more information on the class library, refer to the *DT-Open Layers for .NET Class Library User's Manual*. If you are using the DataAcq SDK or a software application to program your device, refer to the documentation for that software for more information.

The DT9862 Series modules are available either installed in a metal connection box with SMA connectors, or as board-level OEM versions that you can install in your own custom application.

Intended Audience

This document is intended for engineers, scientists, technicians, or others responsible for installing, setting up, using, and/or programming a DT9862 Series module for data acquisition operations.

It is assumed that you are familiar with the requirements of your application. It is also assumed that you have some familiarity with data acquisition principles, that you understand your application, and that you are familiar with the Microsoft® Windows Vista®, Windows 7, or Windows 8 operating system.

How this Manual is Organized

This manual is organized as follows:

- Chapter 1, "Overview," describes the major features of the DT9862 Series module, as well as the supported software and accessories for the module.
- Chapter 2, "Setting Up and Installing the Module," describes how to install a module, how to apply power to the module, and how to configure the device driver.
- Chapter 3, "Wiring Signals," describes how to wire signals to the DT9862 Series module.
- Chapter 4, "Verifying the Operation of a Module," describes how to verify the operation of the module with the Quick DataAcq application.
- Chapter 5, "Principles of Operation," describes all of the features of the module and how to use them in your application.
- Chapter 6, "Supported Device Driver Capabilities," lists the data acquisition subsystems and the associated features accessible using the DT9862 Series Device Driver.

- Chapter 7, "Troubleshooting," provides information that you can use to resolve problems with the module and device driver, should they occur.
- Chapter 8, "Calibration," describes how to calibrate the analog I/O circuitry of the module.
- Appendix A, "Specifications," lists the specifications of the DT9862 Series module.
- Appendix B, "Pin Assignments," describes the pin assignments of the connectors on the DT9862 Series module and STP78 screw terminal panel.
- Appendix C, "Ground, Power, and Isolation," describes the electrical characteristics of the DT9862 Series module.
- An index completes this manual.

Conventions Used in this Manual

The following conventions are used in this manual:

- Notes provide useful information that requires special emphasis, cautions provide information to help you avoid losing data or damaging your equipment, and warnings provide information to help you avoid catastrophic damage to yourself or your equipment.
- Items that you select or type are shown in **bold**.
- `Courier font` is used to represent source code.

Related Information

Refer to the following documents for more information on using the DT9862 Series module:

- *Benefits of the Universal Serial Bus for Data Acquisition.* This white paper describes why USB is an attractive alternative for data acquisition. It is available on the Data Translation® web site (www.datatranslation.com).
- *QuickDAQ User's Manual* (UM-24774). This manual describes how to create a QuickDAQ application to acquire and analyze data from a DT-Open Layers data acquisition module.
- *DT-Open Layers for .NET User's Manual* (UM-22161). For programmers who are developing their own application programs using Visual C# or Visual Basic .NET, this manual describes how to use the DT-Open Layers for .NET Class Library to access the capabilities of Data Translation data acquisition devices.
- *DataAcq SDK User's Manual* (UM-18326). For programmers who are developing their own application programs using the Microsoft C compiler, this manual describes how to use the DT-Open Layers™ DataAcq SDK™ to access the capabilities of Data Translation data acquisition devices. This manual is included on the Data Acquisition OMNI CD.
- *LV-Link Online Help*. This help file describes how to use LV-Link™ with the LabVIEW™ graphical programming language to access the capabilities of Data Translation data acquisition devices.

- *DAQ Adaptor for MATLAB* (UM-22024). This document describes how to use Data Translation's DAQ Adaptor to provide an interface between the MATLAB Data Acquisition subsystem from The MathWorks and Data Translation's DT-Open Layers architecture.
- Microsoft Windows Vista, Windows 7, or Windows 8 documentation.
- USB web site (http://www.usb.org).

Where To Get Help

Should you run into problems installing or using a DT9862 Series module, our Technical Support Department is available to provide technical assistance. Refer to Chapter 7 starting on page 113 for information on how to contact the Technical Support Department. If you are outside the U.S. or Canada, call your local distributor, whose number is listed on Data Translation's web site (www.datatranslation.com).

Overview

DT9862 Series Hardware Features

The DT9862 and DT9862S, shown in Figure 1, are high-speed, multifunction data acquisition modules for the USB (Ver. 2.0 or Ver. 1.1) bus.

Figure 1: DT9862 Series Module

The key hardware features of the DT9862 and DT9862S modules are as follows:

- Available installed in a metal connection box with SMA connectors, or as a board-level OEM version that you can install in your own custom application.
- Simultaneous operation of analog input, analog output, digital I/O, and counter/timer subsystems.
- Analog input subsystem:
  - Two single-ended, simultaneous analog input channels.
  - Throughput rate up to 10.0 MSamples/s when sampling one analog input channel, 5 MS/s when sampling two analog input channels, or 2 MS/s or less when sampling other combination of input channels.
  - The DT9862 provides a bandwidth of 10 MHz. The DT9862S provides a bandwidth of 300 MHz (typical), which allows under-sampling.
  - 16-bit A/D converters.
  - Input range of ±2.5 V for the DT9862 and ±1.25 V for the DT9862S.
  - A 13-location channel list.
  - You can read the digital input port, two 32-bit counters, and three 32-bit quadrature decoders in the analog input data stream.
  - Input samples are stored in memory on the module and are transferred in blocks to the host computer.
- Analog output subsystem:
  - Up to two 16-bit D/A converters (if your module supports analog output channels).
  - Output rate up to 2 MSamples/s (in small steps < 100 mV) or 500 kSamples/s per channel (simultaneous).

  - Output range of ±2.5 V.
  - The analog outputs are deglitched to prevent noise from interfering with the output signal.
  - Output channel list. You can cycle through the output channel list using continuous output mode or waveform generation mode. Waveforms can hold from 2 to 128 kSamples for each analog output channel.
- Digital I/O subsystem:
  - One digital input port, consisting of 16 digital input lines. You can program any of the first eight digital input lines to perform interrupt-on-change operations. You can read the value of the digital input port using the analog input channel-gain list.
  - One digital output port, consisting of 16 digital output lines. You can output the value of the digital output port using the output channel list.
- Two 32-bit counter/timer (C/T) channels that perform event counting, up/down counting, frequency measurement, edge-to-edge measurement, continuous edge-to-edge measurement, continuous pulse output, one-shot, and repetitive one-shot operations. You can read the value of one or more of the C/T channels using the analog input channel list.
- Three 32-bit quadrature decoders that can provide relative or absolute position of quadrature encoder input and calculate rotational speed. You can read the value of one or more of the quadrature decoder channels using the analog input channel list.
- External or internal clock source.
- Trigger operations using a software command, an analog threshold value, or an external digital trigger.
- 500 V galvanic isolation barrier that prevents ground loops to maximize analog signal integrity and protect your computer.

Supported Software

The following software is available for use with the DT9862 Series module and is on the Data Acquisition OMNI CD:

- **DT9862 Series Device Driver** – The device driver allows you to use a DT9862 Series module with any of the supported software packages or utilities. Refer to page 33 for more information on configuring the device driver.
- **Quick DataAcq application** – The Quick DataAcq application provides a quick way to get up and running using a DT9862 Series module. Using this application, you can verify key features of the module, display data on the screen, and save data to disk. Refer to Chapter 4 starting on page 55 for more information on using the Quick DataAcq application.
- **QuickDAQ Base Version** – The base version of QuickDAQ is free-of-charge and allows you to acquire and analyze data from all Data Translation USB and Ethernet devices, except the DT9841 Series, DT9817, DT9835, and DT9853/54. Using the base version of QuickDAQ, you can perform the following functions:
  - Discover and select your devices.
  - Configure all input channel settings for the attached sensors.
  - Load/save multiple hardware configurations.
  - Generate output stimuli (fixed waveforms, swept sine waves, or noise signals).
  - On each supported data acquisition device, acquire data from all channels supported in the input channel list.
  - Choose to acquire data continuously or for a specified duration.
  - Choose software or triggered acquisition.
  - Log acquired data to disk in an .hpf file.
  - Display acquired data during acquisition in either a digital display using the Channel Display window or as a waveform in the Channel Plot window.
  - Choose linear or logarithmic scaling for the horizontal and vertical axes.
  - View statistics about the acquired data, including the minimum, maximum, and mean values and the standard deviation in the Statistics window.
  - Export time data to a .csv or .txt file; you can open the recorded data in Microsoft Excel® for further analysis.
  - Read a previously recorded .hpf data file.
  - Customize many aspects of the acquisition, display, and recording functions to suit your needs, including the acquisition duration, sampling frequency, trigger settings, filter type, and temperature units to use.

- **QuickDAQ FFT Analysis Option** – When enabled with a purchased license key, the QuickDAQ FFT Analysis option includes all the features of the QuickDAQ Base version plus basic FFT analysis features, including the following:
  - The ability to switch between the Data Logger time-based interface and the FFT Analyzer block/average-based interface.
  - Supports software, freerun, or triggered acquisition with accept and reject controls for impact testing applications.
  - Allows you to perform single-channel FFT (Fast Fourier Transform) operations, including AutoSpectrum, Spectrum, and Power Spectral Density, on the acquired analog input data. You can configure a number of parameters for the FFT, including the FFT size, windowing type, averaging type, integration type, and so on.
  - Allows you to display frequency-domain data as amplitude or phase.
  - Supports dB or linear scaling with RMS (root mean squared), peak, and peak-to-peak scaling options
  - Supports linear or exponential averaging with RMS, vector, and peak hold averaging options.
  - Supports windowed time channels.
  - Supports the following response window types: Hanning, Hamming, Bartlett, Blackman, Blackman Harris, and Flat top.
  - Supports the ability to lock the waveform output to the analysis frame time.
  - Allows you to configure and view dynamic performance statistics, including the input below full-scale (IBF), total harmonic distortion (THD), spurious free dynamic range (SFDR), signal-to-noise and distortion ratio (SINAD), signal-to-noise ratio (SNR), and the effective number of bits (ENOB), for selected time-domain channels in the Statistics window.
  - Supports digital IIR (infinite impulse response) filters.
- **QuickDAQ Advanced FFT Analysis Option** – When enabled with a purchased software license, the QuickDAQ Advanced FFT Analysis option includes all the features of the QuickDAQ Base version with the FFT Analysis option plus advanced FFT analysis features, including the following:
  - Allows you to designate a channel as a Reference or Response channel.
  - Allows you to perform two-channel FFT analysis functions, including Frequency Response Functions (Inertance, Mobility, Compliance, Apparent Mass, Impedance, Dynamic Stiffness, or custom FRF) with H1, H2, or H3 estimator types, Cross-Spectrum, Cross Power Spectral Density, Coherence, and Coherent Output Power.
  - Supports the Exponential response window type.
  - Supports the following reference window types: Hanning, Hamming, Bartlett, Blackman, Blackman Harris, FlatTop, Exponential, Force, and Cosine Taper windows.
  - Supports real, imaginary, and Nyquist display functions.
  - Allows you to save data in the .uff file format.

- **DT-Open Layers for .NET Class Library** – Use this class library if you want to use Visual C# or Visual Basic for .NET to develop your own application software for a DT9862 Series module using Visual Studio 2003 to 2012; the class library complies with the DT-Open Layers standard.
- **DataAcq SDK** – Use the Data Acq SDK if you want to use Visual Studio 6.0 and Microsoft C or C++ to develop your own application software for a DT9862 Series module using Windows Vista, Windows 7, or Windows 8; the DataAcq SDK complies with the DT-Open Layers standard.
- **DAQ Adaptor for MATLAB** – Data Translation's DAQ Adaptor provides an interface between the MATLAB Data Acquisition (DAQ) subsystem from The MathWorks and Data Translation's DT-Open Layers architecture.
- **LV-Link** – A link to LV-Link is included on the Data Acquisition OMNI CD. Use LV-Link if you want to use the LabVIEW graphical programming language to access the capabilities of Data Translation modules.

Refer to the Data Translation web site (www.datatranslation.com) for information about selecting the right software package for your needs.

Accessories

Table 1 lists the following optional accessories for use with the DT9862 Series modules.

Table 1: Accessories for the DT9862 Series Module

Accessory		Description
STP78		Screw terminal panel for connecting digital signals to the DT9862 Series module. Use this panel with the EP390 cable.
EP390		A 1.52 meter cable with two 78-pin connectors that connect the STP78 screw terminal panel to the DT9862 Series module.
EP361		+5 V power supply and cable. EP361 is shipped with the standard version of the DT9862 Series module. If you purchased the OEM version of the module, EP361 is optional.

Getting Started Procedure

The flow diagram shown in Figure 2 illustrates the steps needed to get started using the DT9862 Series module. This diagram is repeated in each Getting Started chapter; the shaded area in the diagram shows you where you are in the procedure.

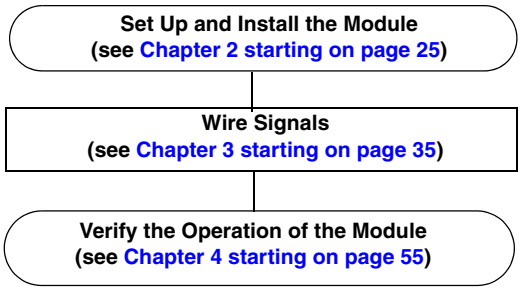
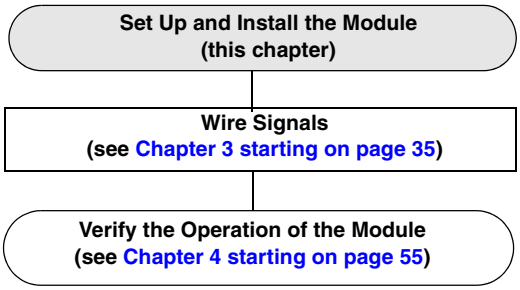


Figure 2: Getting Started Flow Diagram

Part 1: Getting Started

Setting Up and Installing the Module



Note: DT9862 Series modules are factory-calibrated. If you decide that you want to recalibrate the analog input or analog output circuitry, refer to the instructions in Chapter 8.

Unpacking

Open the shipping box and verify that the following items are present:

- DT9862 Series module
- Data Acquisition OMNI CD
- USB cable
- EP361 power supply and power cable

Note: If you purchased the OEM version of the DT9862 Series, the USB cable and EP361 power supply and cable are not shipped with the module.

If an item is missing or damaged, contact Data Translation. If you are in the United States, call the Customer Service Department at (508) 481-3700, ext. 1323. An application engineer will guide you through the appropriate steps for replacing missing or damaged items. If you are located outside the United States, call your local distributor, listed on Data Translation's web site (www.datatranslation.com).

System Requirements

For reliable operation, ensure that your computer meets the following system requirements:

- Processor: Pentium 4/M or equivalent
- RAM: 1 GB
- Screen Resolution: 1024 x 768 pixels
- Operating System: Windows 8, Windows 7, or Windows Vista (32- and 64-bit)
- Disk Space: 4 GB

Applying Power to the Module

The standard DT9862 and DT9862S modules are shipped with an EP361 +5V power supply and cable. For the OEM version of the DT9862 and DT9862S modules, you must provide your own +5 V power source or purchase the EP361 power supply and cable from Data Translation.

To apply power to the module, do the following:

1. Connect the +5 V power supply to the power connector on the DT9862 or DT9862S module. Refer to Figure 3.

Figure 3: Attaching a +5 V Power Supply to the DT9862 Series Module

2. Plug the power supply into a wall outlet.

For more detailed information about ground, power, and isolation connections on a DT9862 Series module, refer to Appendix C starting on page 149.

Attaching Modules to the Computer

This section describes how to attach DT9862 Series modules to the host computer.

Note: Most computers have several USB ports that allow direct connection to USB devices. If your application requires more DT9862 Series modules than you have USB ports for, you can expand the number of USB devices attached to a single USB port by using expansion hubs. For more information, refer to page 31.

You can unplug a module, then plug it in again, if you wish, without causing damage. This process is called hot-swapping. Your application may take a few seconds to recognize a module once it is plugged back in.

You must install the device driver before connecting your DT9862 Series module(s) to the host computer. Run the installation program on your Data Acquisition OMNI CD to install the device driver and other software for the module.

Connecting Directly to the USB Ports

To connect a DT9862 Series module directly to a USB port on your computer, do the following:

1. Make sure that you have attached a power supply to the module.
2. Attach one end of the USB cable to the USB port on the module.
3. Attach the other end of the USB cable to one of the USB ports on the host computer, as shown in Figure 4.
   The operating system automatically detects the USB module and starts the Found New Hardware wizard.

Figure 4: Attaching the USB Cable to the DT9862 Series Module

4. *For Windows Vista*:
   a. Click **Locate and install driver software (recommended)**.
      The popup message "Windows needs your permission to continue" appears.
   b. Click **Continue**.
      The Windows Security dialog box appears.
   c. Click **Install this driver software anyway**.
      The LED on the module turns green.

Note: Windows 7 and Windows 8 find the device automatically.

5. Repeat these steps to attach another DT9862 Series module to the host computer, if desired.

Connecting to an Expansion Hub

Expansion hubs are powered by their own external power supply. The practical number of DT9862 Series modules that you can connect to a single USB port depends on the throughput you want to achieve.

To connect multiple DT9862 Series modules to an expansion hub, do the following:

1. Make sure that you have attached a power supply to the module.
2. Attach one end of the USB cable to the module and the other end of the USB cable to an expansion hub.
3. Connect the power supply for the expansion hub to an external power supply.
4. Connect the expansion hub to the USB port on the host computer using another USB cable.
   The operating system automatically detects the USB module and starts the Found New Hardware wizard.
5. *For Windows Vista*:
   a. Click **Locate and install driver software (recommended)**.
      The popup message "Windows needs your permission to continue" appears.
   b. Click **Continue**.
      The Windows Security dialog box appears.
   c. Click **Install this driver software anyway**.
      The LED on the module turns green.

Note: Windows 7 and Windows 8 find the device automatically.

6. Repeat these steps until you have attached the number of expansion hubs and modules that you require. Refer to Figure 5.
   The operating system automatically detects the USB devices as they are installed.

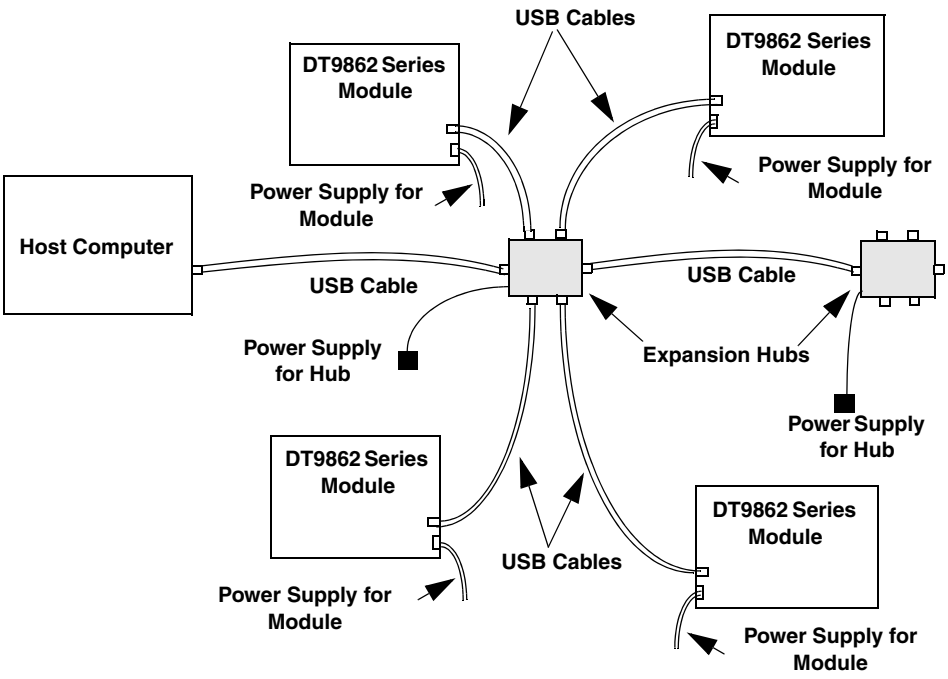


Figure 5: Attaching Multiple Modules Using Expansion Hubs

Configuring the DT9862 Series Device Driver

Note: In Windows 7, Windows 8, and Vista, you must have administrator privileges to run the Open Layers Control Panel. When you double-click the Open Layers Control Panel icon, you may see the Program Compatibility Assistant. If you do, select **Open the control panel using recommended settings**. You may also see a Windows message asking you if you want to run the Open Layers Control Panel as a "legacy CPL elevated." If you get this message, click **Yes**.

If you do not get this message and have trouble making changes in the Open Layers Control Panel, right click the DTOLCPL.CPL file and select **Run as administrator**. By default, this file is installed in the following location:

Windows 7, Windows 8, and Vista (32-bit)
C:\Windows\System32\Dtolcpl.cpl

Windows 7, Windows 8, and Vista (64-bit)
C:\Windows\SysWOW64\Dtolcpl.cpl

To configure the device driver for the DT9862 Series modules, do the following:

1. If you have not already done so, power up the host computer and all peripherals.
2. From the Windows Start menu, select **Settings | Control Panel**.
3. From the Control Panel, double-click **Open Layers Control Panel**.
   The Data Acquisition Control Panel dialog box appears.
4. Click the DT9862 Series module that you want to configure, and then click **Advanced**.
   The Configurable Board Options dialog box appears.
5. If required, select the digital input line(s) that you want to use for interrupt-on-change operations. When any of the selected lines changes state, the module reads the entire digital input value and generates an interrupt.
6. If you are using USB 2.0, check the **USB Version 2.0** checkbox to improve performance.
7. If you want to use the internal 50 Ω termination that the DT9862 module provides to match the impedance of your cable, check the **Channel 0** checkbox to use the internal termination on analog input channel 0 and/or check the **Channel 1** checkbox to use the internal termination on analog input channel 1. Refer to page 37 for more information on cable matching.

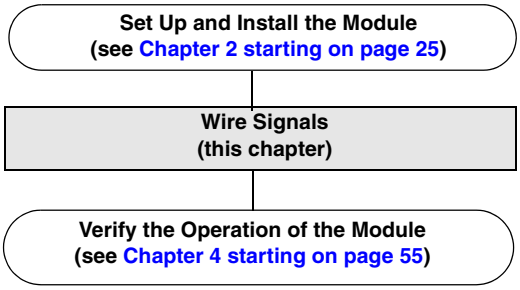
   Note: You can also change this setting programmatically, if desired, by writing to a register on the module; refer to page 153 for more information.

   The DT9862S does not provide 50 Ω of termination on the inputs; therefore, you must provide your own external termination at the end of the cable. Refer to page 37 for more information on cable matching.

8. Click **OK**.
9. If you want to rename the module, click **Edit Name**, enter a new name for the module, and then click **OK**. The name is used to identify the module in all subsequent applications.
10. Repeat steps 4 to 9 for the other modules that you want to configure.
11. When you are finished configuring the modules, click **Close**.

Continue with the instructions on wiring in Chapter 3.

Wiring Signals


Set Up and Install the Module
(see Chapter 2 starting on page 25)
Wire Signals
(this chapter)
Verify the Operation of the Module
(see Chapter 4 starting on page 55)

Preparing to Wire Signals

This section provides recommendations and information about wiring signals to the DT9862 Series module.

Wiring Recommendations

Keep the following recommendations in mind when wiring signals to the DT9862 Series module:

- Follow standard ESD procedures when wiring signals to the module.
- Separate power and signal lines by using physically different wiring paths or conduits.
- To avoid noise, do not locate the box and cabling next to sources that produce high electromagnetic fields, such as large electric motors, power lines, solenoids, and electric arcs, unless the signals are enclosed in a mumetal shield.
- Prevent electrostatic discharge to the I/O while the box is operational.
- Connect all unused analog input channels to analog ground.

High-Performance Considerations

Cables have a characteristic impedance that must be matched or amplitude and phase errors will result in poor data. For optimal performance, particularly at high frequencies, do the following:

- Pay attention to cable matching from the source to the analog input channels of the DT9862 Series module.
- Place a resistor with the same impedance in series with the cable at your source.
- Add termination with matched impedance at the module.

  The DT9862 provides 50 Ω of internal termination that you can select for each analog input channel using the Control Panel applet; refer to page 33 for more information. Alternatively, you can provide your own external termination.

  The DT9862 does not provide 50 Ω of input termination; therefore, you must provide your own external termination at the end of the cable (use a T connector to do this).
- At frequencies of 10 MHz and above, connect the shield all the way through.

The following example assumes that your cable has an impedance of 50 Ω. You can place a 50 Ω resistor in series with a 1000 pF NPO capacitor to common, as shown in Figure 6. This will provide high frequency matching without DC loading of the termination resistor.

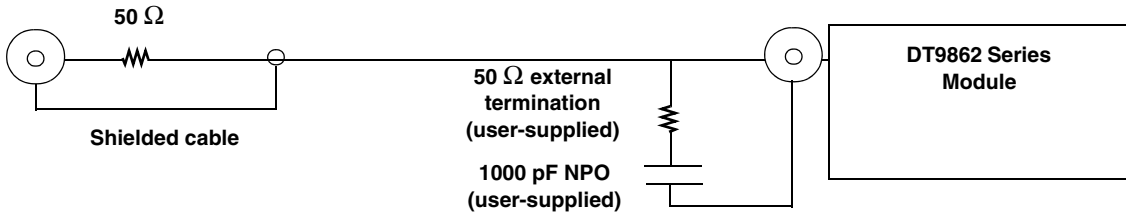


Figure 6: Example of Cable Matching

Layout of the DT9862 Series Module

The DT9862 Series module contains SMA connectors and a 78-pin, I/O connector for connecting digital I/O, counter/timer, and quadrature decoder signals. Figure 7 shows the I/O connectors on the front of the DT9862 Series module, and Figure 8 shows the I/O connectors on the rear of the DT9862 Series module.

Figure 7: I/O Connectors on the Front of the DT9862 Series Module

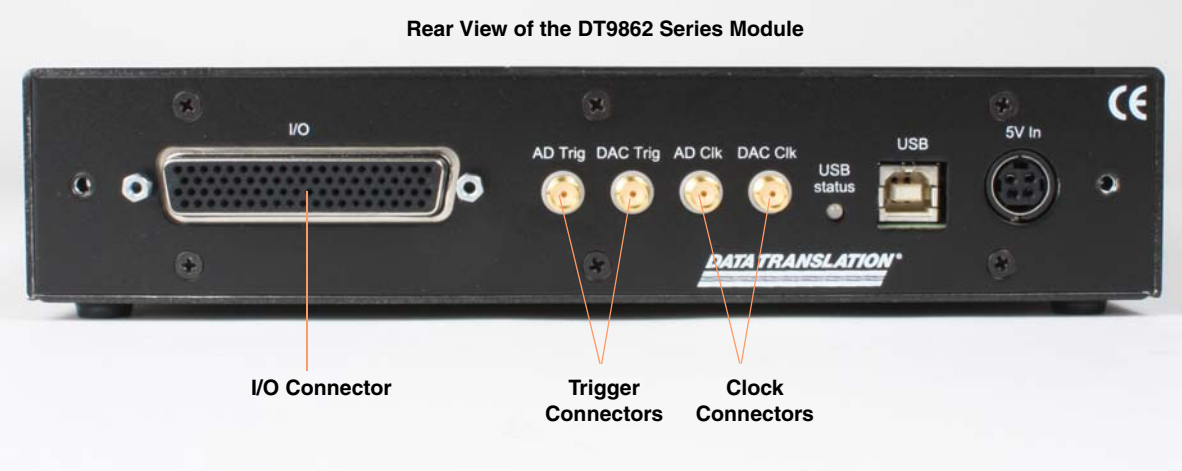


Figure 8: I/O Connectors on the Rear of the DT9862 Series Module

You can wire the following I/O signals to the DT9862 Series module:

- **Analog input signals** – Wire analog input signals using the SMA connectors labelled Ain Ch0 and Ain Ch1.
- **Analog output signals** – Wire analog output signals using the SMA connectors labelled D/A Out Ch0 and D/A Out Ch1.
- **Digital I/O signals** – To wire digital I/O signals, you must use the appropriate pins on the I/O connector on the DT9862 Series module. You can access the pins by using the STP78 screw terminal panel and EP390 cable or by building your own cable/panel. Refer to page 146 for connector pin assignments.
- **Counter/timer signals** – To wire counter/timer signals, you must use the appropriate pins on the I/O connector on the DT9862 Series module. You can access the pins by using the STP78 screw terminal panel and EP390 cable or by building your own cable/panel. Refer to page 146 for connector pin assignments.
- **External A/D clock or trigger signal** – You can wire external clock/trigger signals for the analog input subsystem using the SMA connectors labelled AD Clk for A/D clock signals and AD Trig for A/D trigger signals.
- **External D/A clock or trigger signal** – You can wire external clock/trigger signals for the analog output subsystem using the SMA connectors labelled DAC Clk for D/A clock signals and DAC Trig for D/A trigger signals.

The following sections describe how to wire signals to a DT9862 Series module.

Wiring Analog Input Signals

The DT9862 Series supports voltage inputs. You can connect analog input signals to the DT9862 Series modules in **single-ended** mode. In this mode, the source of the input should be close to the module; all the input signals are referred to the same common ground.

Figure 9 shows how to connect voltage inputs (channels 0 and 1, in this case) to the SMA connectors on a DT9862 Series module.

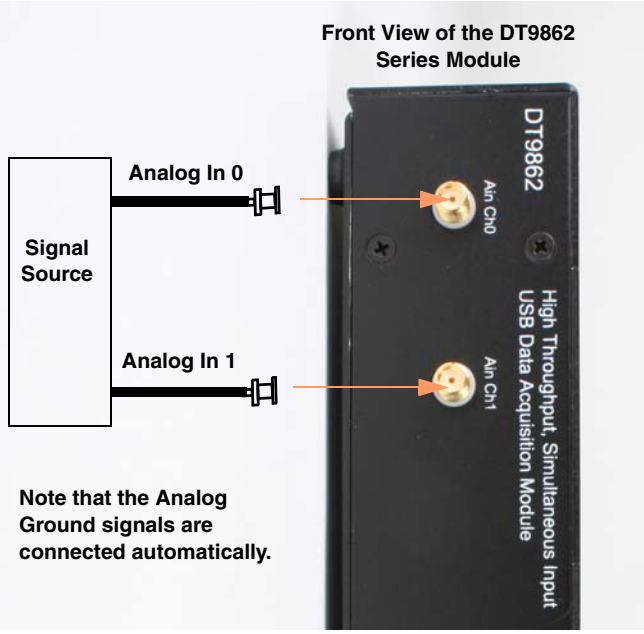


Figure 9: Wiring Analog Inputs to a DT9862 Series Module

Wiring Analog Output Signals

Figure 10 shows how to connect an analog output voltage signal (channel 1, in this case) to the SMA connector on a DT9862 Series module.

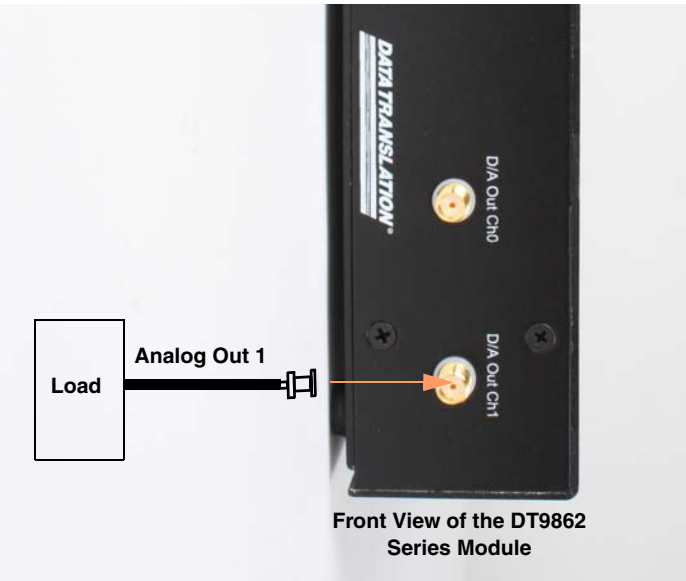


Figure 10: Wiring Analog Outputs to a DT9862 Series Module

Wiring Signals to the I/O Connector

If want to connect digital, counter/timer, or quadrature decoder signals to a DT9862 Series module, it is recommended that you connect an STP78 screw terminal panel to the 78-pin, D-sub, I/O connector on the module. Alternatively, you can build your own screw terminal panel and cable.

Figure 11 shows how to connect the STP78 screw terminal panel to the I/O connector using the EP390 cable.

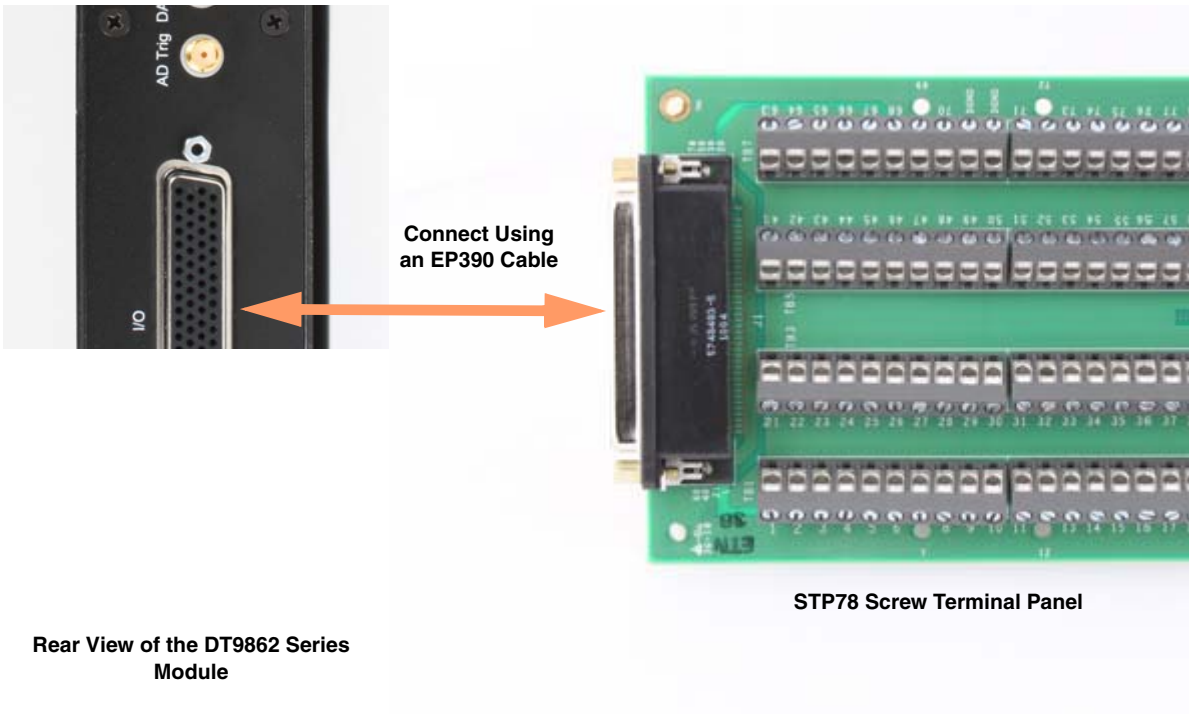


Figure 11: Connecting the STP78 Screw Terminal Panel to a DT9862 Series Module

Figure 12 shows the screw terminal designations for the STP78 screw terminal panel.

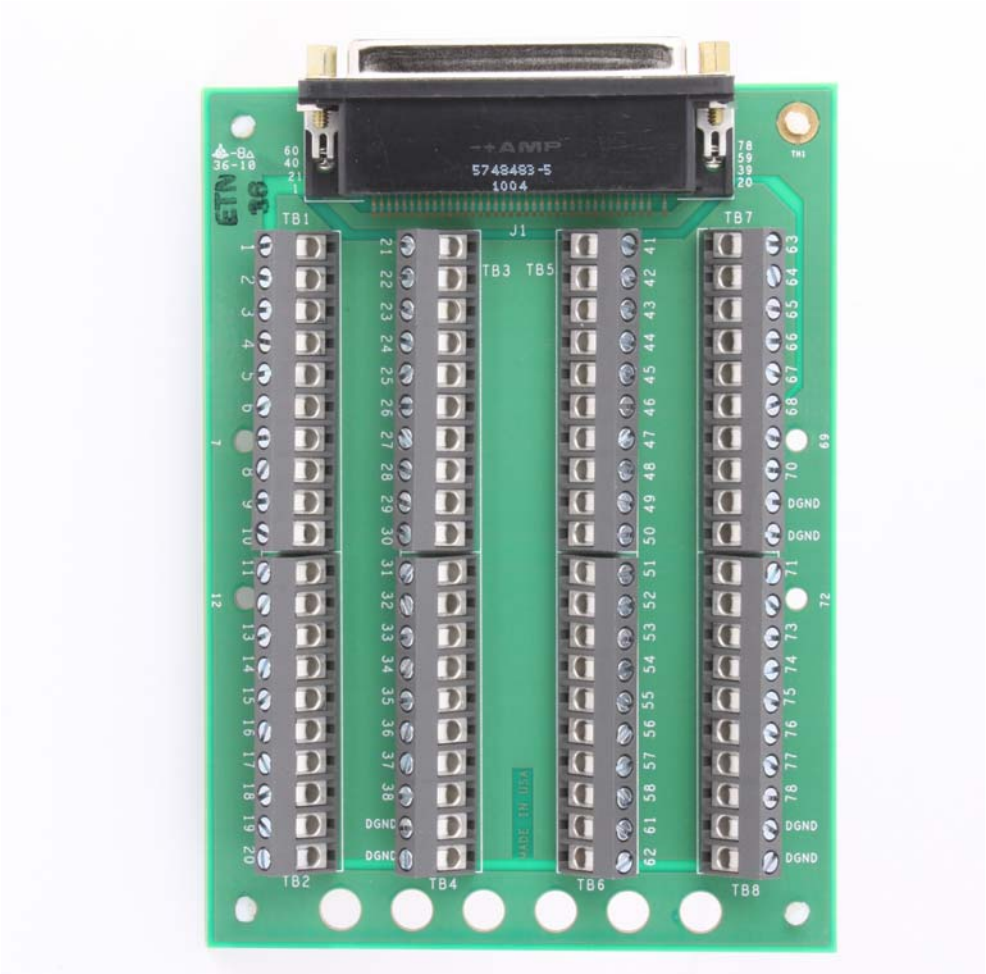


Figure 12: Layout of the STP78

Table 2 lists the assignments for each screw terminal on the STP78 screw terminal panel.

Table 2: Screw Terminal Assignments for the STP78 Screw Terminal Panel

Screw Terminal	Terminal Block Position	Signal Description	Screw Terminal	Terminal Block Position	Signal Description
1	TB1, 10	Quad Dec 1 Index	41	TB5, 1	Digital Output 0
2	TB1, 9	Digital Ground	42	TB5, 2	Digital Output 1
3	TB1, 8	Quad Dec 1 B	43	TB5, 3	Digital Output 2
4	TB1, 7	Digital Ground	44	TB5, 4	Digital Output 3
5	TB1, 6	Quad Dec 1 A	45	TB5, 5	Digital Output 4
6	TB1, 5	Digital Ground	46	TB5, 6	Digital Output 5
7	TB1, 4	Quad Dec 0 Index	47	TB5, 7	Digital Output 6
8	TB1, 3	Digital Ground	48	TB5, 8	Digital Output 7
9	TB1, 2	Quad Dec 0 B	49	TB5, 9	Digital Output 8
10	TB1, 1	Digital Ground	50	TB5, 10	Digital Output 9
11	TB2, 10	Quad Dec 0 A	51	TB6, 1	Digital Output 10
12	TB2, 9	Digital Ground	52	TB6, 2	Digital Output 11
13	TB2, 8	Counter 0 Out	53	TB6, 3	Digital Output 12
14	TB2, 7	Digital Ground	54	TB6, 4	Digital Output 13
15	TB2, 6	Counter 0 Gate	55	TB6, 5	Digital Output 14
16	TB2, 5	Digital Ground	56	TB6, 6	Digital Output 15
17	TB2, 4	Counter 0 Clock	57	TB6, 7	Digital Ground
18	TB2, 3	Digital Ground	58	TB6, 8	Digital Ground
19	TB2, 2	+5 V Output	59	TB6, 9	Digital Input 0
20	TB2, 1	+5 V Output Ground	60	TB6, 10	Digital Input 1
21	TB3, 10	Quad Dec 2 Index	61	TB7, 1	Digital Input 2
22	TB3, 9	Digital Ground	62	TB7, 2	Digital Input 3
23	TB3, 8	Quad Dec 2 B	63	TB7, 3	Digital Input 4
24	TB3, 7	Digital Ground	64	TB7, 4	Digital Input 5
25	TB3, 6	Quad Dec 2 A	65	TB7, 5	Digital Input 6
26	TB3, 5	Digital Ground	66	TB7, 6	Digital Input 7
27	TB3, 4	Counter 1 Output	67	TB7, 7	Digital Input 8
28	TB3, 3	Digital Ground	68	TB7, 8	Digital Input 9
29	TB3, 2	Counter 1 Gate	69	TB7, 9	Digital Ground
30	TB3, 1	Digital Ground	70	TB7, 10	Digital Ground

Table 2: Screw Terminal Assignments for the STP78 Screw Terminal Panel (cont.)

Screw Terminal	Terminal Block Position	Signal Description	Screw Terminal	Terminal Block Position	Signal Description
31	TB4, 10	Counter 1 Clock	71	TB8, 1	Digital Input 10
32	TB4, 9	Digital Ground	72	TB8, 2	Digital Input 11
33	TB4, 8	Reserved	73	TB8, 3	Digital Input 12
34	TB4, 7	Reserved	74	TB8, 4	Digital Input 13
35	TB4, 6	Reserved	75	TB8, 5	Digital Input 14
36	TB4, 5	Reserved	76	TB8, 6	Digital Input 15
37	TB4, 4	Reserved	77	TB8, 7	Digital Ground
38	TB4, 3	Reserved	78	TB8, 8	Digital Ground
39	TB4, 2	Digital Ground	79	TB8, 9	Digital Ground
40	TB4, 1	Digital Ground	80	TB8, 10	Digital Ground

The following subsections describe how to connect digital I/O, counter/timer, and quadrature decoder signals to the STP78 screw terminal panel.

Wiring Digital I/O Signals

Figure 13 shows how to connect digital input signals (lines 0 and 1, in this case) to the STP78 screw terminal panel.

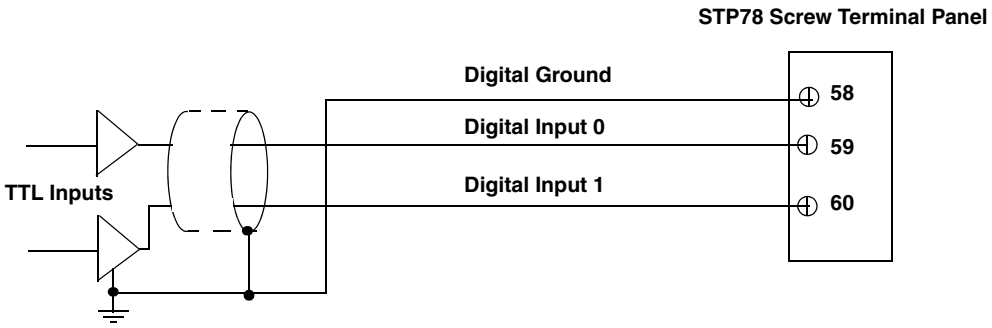


Figure 13: Wiring Digital Inputs to the STP78 Screw Terminal Panel

Figure 14 shows how to connect a digital output (line 0, in this case) to the digital output pins of the I/O connector.

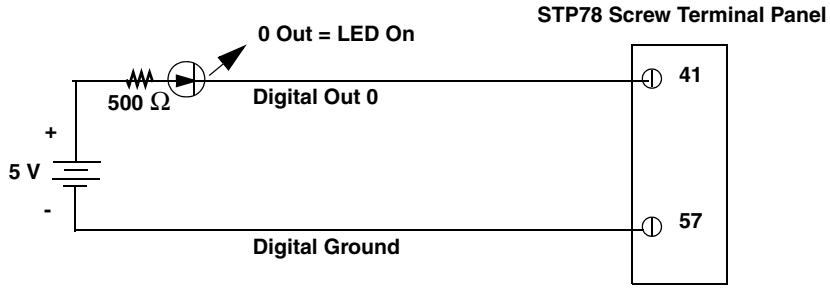


Figure 14: Wiring Digital Outputs to the STP78 Screw Terminal Panel

Wiring Counter/Timer Signals

The DT9862 Series module provides two counter/timer channels that you can use for the following operations:

- Event counting
- Up/down counting
- Frequency measurement
- Pulse width/period measurement
- Edge-to-edge measurement
- Continuous edge-to-edge measurement
- Pulse output (continuous, one-shot, and repetitive one-shot)

This section describes how to connect counter/timer signals to the STP78 screw terminal panel. Refer to Chapter 5 for more information about using the counter/timers. Refer to page 146 for more information about the STP78 screw terminal panel.

Event Counting

Figure 15 shows how to connect counter/timer signals to perform an event counting operation on counter/timer 0 using an external gate.

The counter counts the number of rising edges that occur on the Counter 0 Clock input when the Counter 0 Gate signal is in the active state (as specified by software). Refer to page 47 for more information on event counting operations.

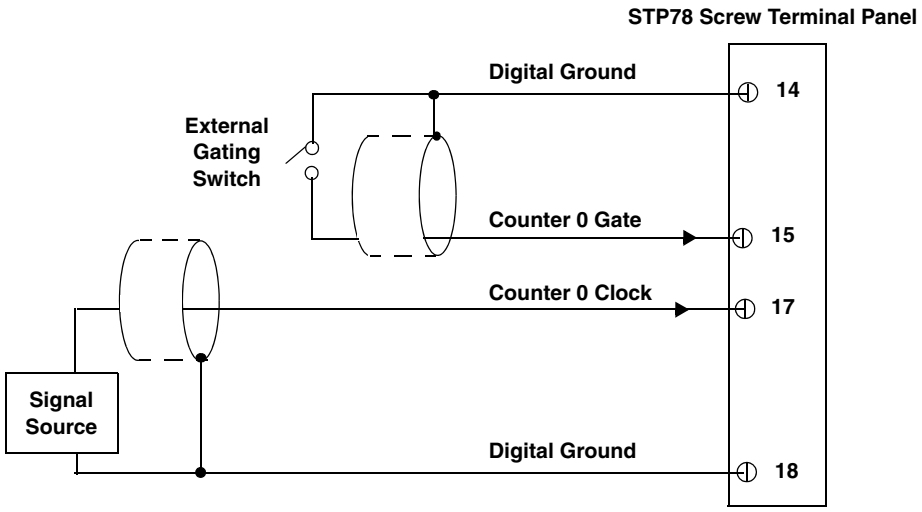


Figure 15: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for an Event Counting Operation Using an External Gate

Figure 16 shows how to connect counter/timer signals to perform an event counting operation on counter/timer 0 without using a gate. The counter counts the number of rising edges that occur on the Counter 0 Clock input.

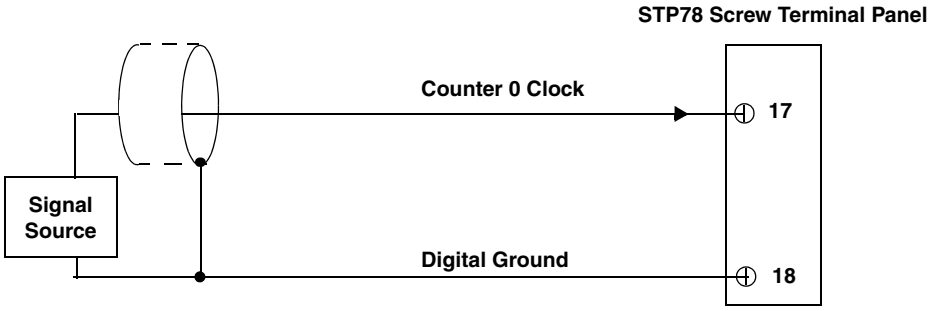


Figure 16: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for an Event Counting Operation Without Using a Gate

Up/Down Counting

Figure 17 shows how to connect counter/timer signals to perform an up/down counting operation on counter/timer 0. The counter keeps track of the number of rising edges that occur on the Counter 0 Clock input. The counter increments when the Counter 0 Gate signal is high and decrements when the Counter 0 Gate signal is low. Refer to page 91 for more information about up/down counting operations.

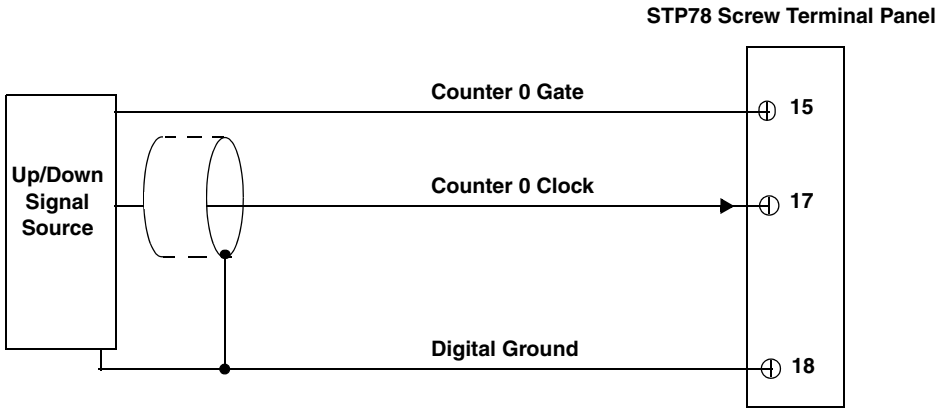


Figure 17: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for an Up/Down Counting Operation

Frequency Measurement

One way to measure frequency is to connect a pulse of a known duration (such as a one-shot output of counter/timer 1) to the Counter 0 Gate input.

Figure 18 shows how to connect counter/timer signals to perform a frequency measurement operation. In this case, the frequency of the Counter 0 clock input is the number of counts divided by the period of the Counter 0 Gate input signal. Refer to page 91 for more information about frequency measurement operations.

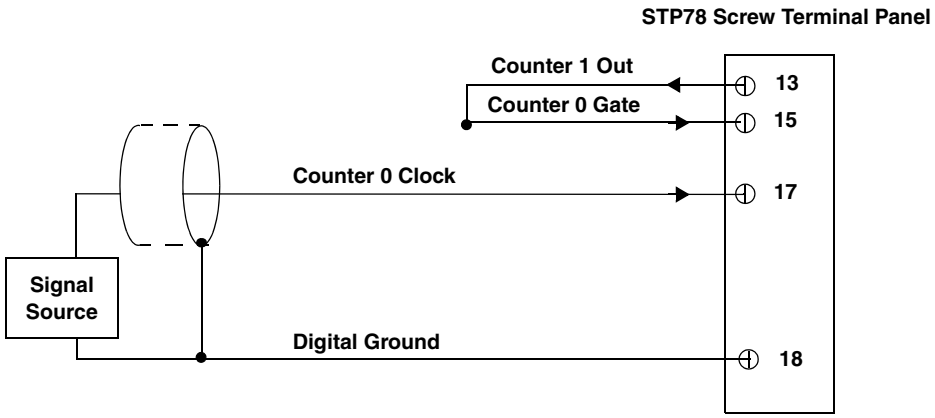


Figure 18: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for a Frequency Measurement Operation Using an External Pulse

Period/Pulse Width Measurement

Figure 19 shows how to connect counter/timer signals to perform a period/pulse width measurement operation on counter/timer 0. You specify the active pulse (high or low) in software. The pulse width is the percentage of the total pulse period that is active. Refer to page 90 for more information about pulse periods and pulse widths.

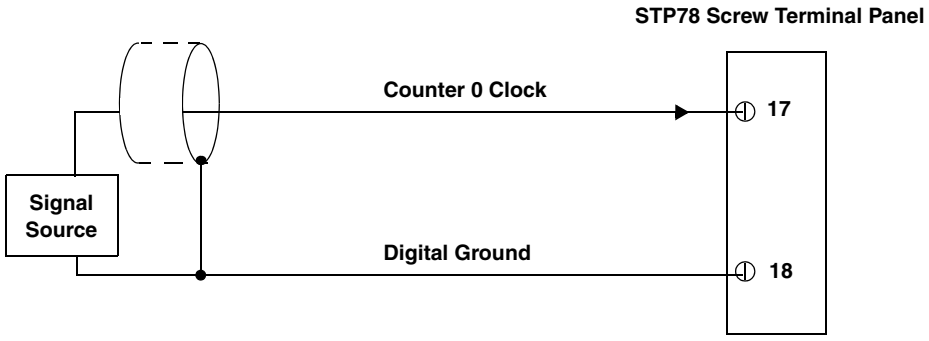


Figure 19: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for a Period/Pulse Width Measurement Operation

Edge-to-Edge Measurement

Figure 20 shows how to connect counter/timer signals to perform an edge-to-edge measurement operation using two signal sources. The counter measures the number of counts between the start edge (in this case, a rising edge on the Counter 0 Clock signal) and the stop edge (in this case, a falling edge on the Counter 0 Gate signal).

You specify the start edge and the stop edge in software. Refer to page 92 for more information on edge-to-edge measurement mode.

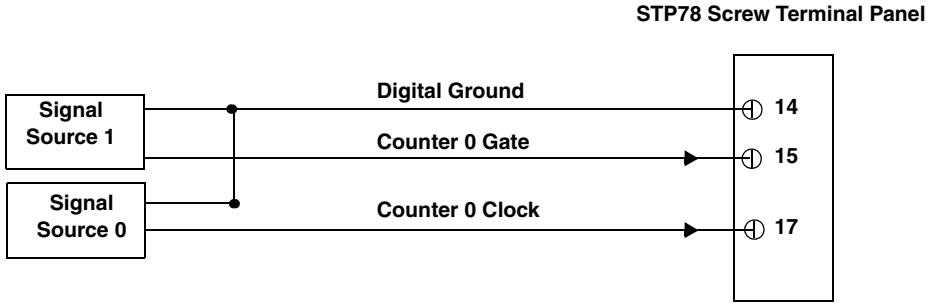


Figure 20: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for an Edge-to-Edge Measurement Operation

Continuous Edge-to-Edge Measurement

Figure 21 shows how to connect counter/timer signals to perform a continuous edge-to-edge measurement operation. The counter measures the number of counts between two consecutive start edges (in this case, a rising edge on the Counter 0 Clock signal).

You specify the start edge in software. Refer to page 93 for more information on continuous edge-to-edge measurement operations.

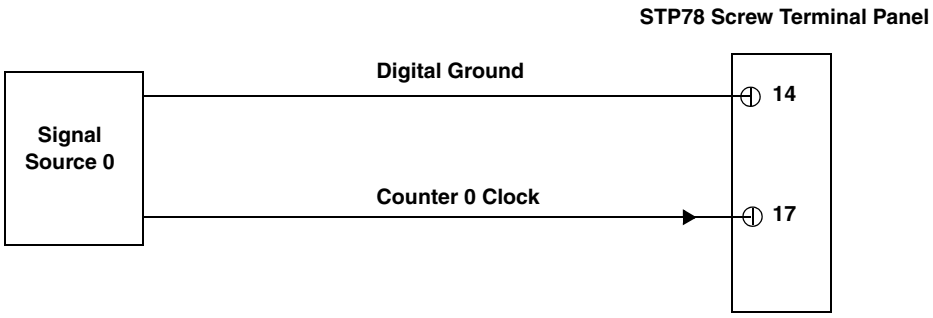


Figure 21: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for a Continuous Edge-to-Edge Measurement Operation

Pulse Output

Figure 22 shows how to connect counter/timer signals to perform a pulse output operation on counter/timer 0; in this example, an external gate is used. Refer to page 52 for more information on pulse output operations.

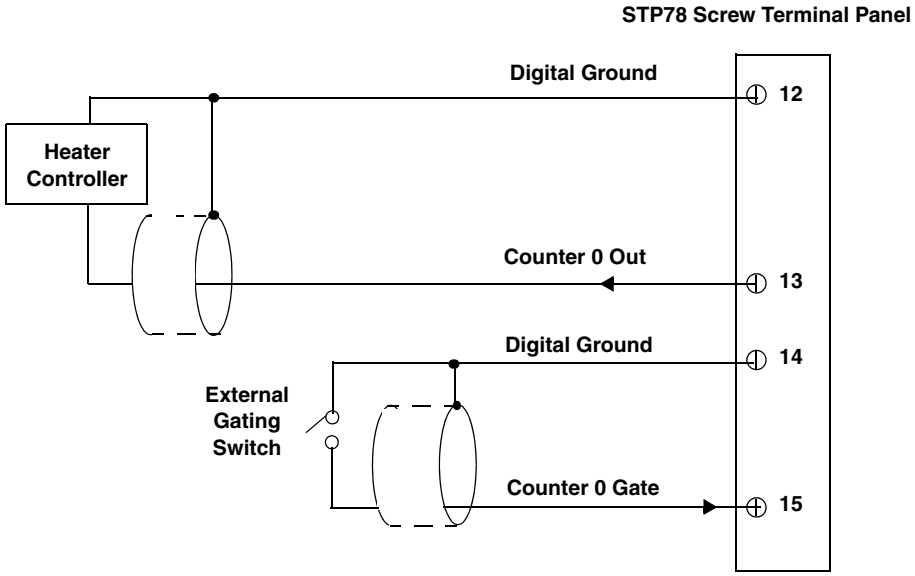


Figure 22: Wiring Counter/Timer Signals to the STP78 Screw Terminal Panel for a Pulse Output Operation Using an External Gate

Wiring Quadrature Decoder Signals

The DT9862 Series modules provide three quadrature decoder channels that allow simultaneous decoding of three quadrature encoded inputs.

Each quadrature decoder supports "A," "B," and "Index" inputs and is used to interface with a quadrature encoder sensor. The A and B input relationships are used to increment or decrement the positional count; the Index input can be used to zero-out the positional count. Refer to page 96 for more information about using the quadrature decoders.

Figure 23 shows how to connect signals from a quadrature encoder to quadrature decoder 0 on the STP78 screw terminal panel.

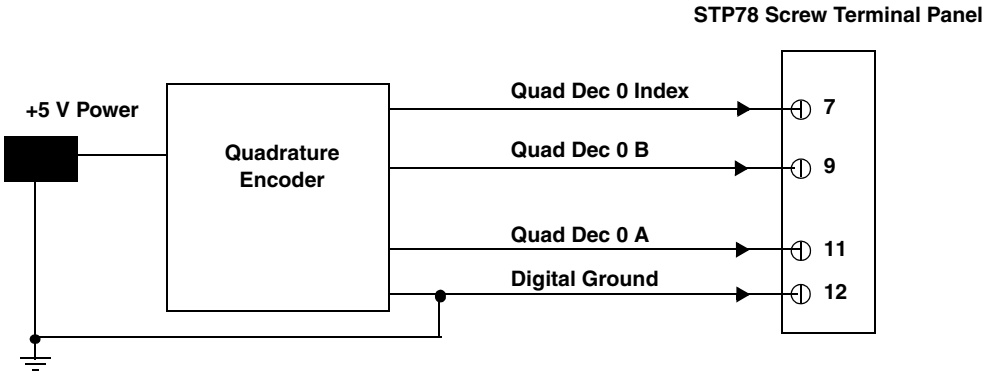
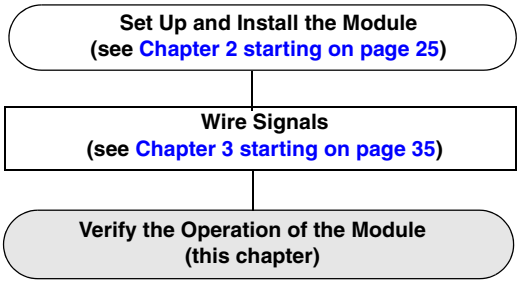


Figure 23: Wiring Quadrature Decoder Signals to the STP78 Screw Terminal Panel

Verifying the Operation of a Module



You can verify the operation of a DT9862 Series module using the Quick DataAcq application. Quick DataAcq lets you do the following:

- Acquire data from a single analog input channel or digital input port
- Acquire data continuously from one or more analog input channels using an oscilloscope, strip chart, or Fast Fourier Transform (FFT) view
- Measure the frequency of events
- Output data from a single analog output channel or digital output port
- Output pulses either continuously or as a one-shot
- Save the input data to disk

Running the Quick DataAcq Application

The Quick DataAcq application is installed automatically when you install the driver software.

To run the Quick DataAcq application, do the following:

1. If you have not already done so, power up your computer and any attached peripherals.
2. Click **Start** from the Task Bar.
3. Browse to **Programs | Data Translation, Inc | DT-Open Layers for Win32 | QuickDataAcq**.
   The main menu appears.

Note: The Quick DataAcq application allows you to verify basic operations on the module; however, it may not support all of the module's features.

For information on each of the features provided, use the online help for the Quick DataAcq application by pressing F1 from any view or selecting the **Help** menu. If the system has trouble finding the help file, navigate to C:\Program Files\Data Translation\Win32\dtdataacq.hlp, where C: is the letter of your hard disk drive.

Testing Single-Value Analog Input

To verify that the module can read a single analog input value, do the following:

1. Connect a voltage source, such as a function generator, to analog input channel 0 on the DT9862 Series module. Refer to page 40 for an example of how to connect an analog input.
2. In the Quick DataAcq application, choose **Single Analog Input** from the **Acquisition** menu.
3. Select the appropriate DT9862 Series module from the **Board** list box.
4. In the **Channel** list box, select analog input channel 0.
5. In the **Range** list box, select the range for the channel.
6. Select **Single Ended**.
7. Click **Get** to acquire a single value from analog input channel 0.
   The application displays the value on the screen in both text and graphical form.

Testing Single-Value Analog Output

To verify that the module can output a single analog output value, do the following:

1. Connect an oscilloscope or voltmeter to analog output channel 0 on the module. Refer to page 41 for an example of how to connect analog output signals.
2. In the Quick DataAcq application, choose **Single Analog Output** from the **Control** menu.
3. Select the appropriate DT9862 Series module from the **Board** list box.
4. In the **Channel** list box, select analog output channel 0.
5. In the **Range** list box, select the output range of DAC0.
6. Enter an output value, or use the slider to select a value, to output from DAC0.
7. Click **Send** to output a single value from analog output channel 0.
   The application displays the output value both on the slider and in the text box.

Testing Continuous Analog Input

To verify that the module can perform a continuous analog input operation, do the following:

1. Connect known voltage sources, such as the outputs of a function generator, to analog input channels 0 and 1 on the DT9862 Series module.
2. In the Quick DataAcq application, choose **Scope** from the **Acquisition** menu.
3. Select the DT9862 Series module from the **Board** list box.
4. In the **Sec/Div** list box, select the number of seconds per division (.1 to .00001) for the display.
5. In the **Channel** list box, select analog input channel 1, and then click **Add** to add the channel to the channel list. *Note that, by default, channel 0 is included in the channel list*.
6. Click **Config** from the Toolbar.
7. In the **Config** dialog, select **ChannelType**, and then select **Single Ended**.
8. In the **Config** dialog, select **Range,** and then select **Bipolar**.
9. Click **OK** to close the dialog box.
10. In the **Trigger** box, select **Auto** to acquire data continuously from the specified channels or **Manual** to acquire a burst of data from the specified channels.
11. Click **Start** from the Toolbar to start the continuous analog input operation.
    The application displays the values acquired from each channel in a unique color on the oscilloscope view.
12. Click **Stop** from the Toolbar to stop the operation.

Testing Single-Value Digital Input

To verify that the module can read a single digital input value, do the following:

1. Connect a digital input to digital input line 0 on the DT9862 Series module. Refer to page 46 for information about how to connect a digital input.
2. In the Quick DataAcq application, choose **Digital Input** from the **Acquisition** menu.
3. Select the appropriate DT9862 Series module from the **Board** list box.
4. Click **Get**.
   The application displays the entire 16-bit digital input value (0 to FFFF) in both the Data box and the Digital Input box.

   In addition, application shows the state of the lower eight digital input lines (lines 0 to 7) in the graphical display. If an indicator light is lit (red), the line is high; if an indicator light is not lit (black), the line is low.

Note: Although the DT9862 Series module contains 16 digital input lines, the Quick DataAcq application shows indicator lights for the lower eight digital input lines only. The 16-bit value is the correct value for all 16 lines.

Testing Single-Value Digital Output

Note: Although the DT9862 Series modules contain 16 digital output lines, the Quick DataAcq application allows you to perform a digital output operation on the lower eight digital output lines (lines 0 to 7) only.

To verify that the module can output a single digital output value, do the following:

1. Connect a digital output to digital output line 0 on the DT9862 Series module. Refer to page 46 for information about how to connect a digital output.
2. In the Quick DataAcq application, choose **Digital Output** from the **Control** menu.
3. Select the appropriate DT9862 Series module from the **Board** list box.
4. Click the appropriate indicator lights to select the types of signals to write from the digital output lines. If you select a light, the module outputs a high-level signal; if you do not select a light, the module outputs a low-level signal. You can also enter an output value for the lower eight digital output lines (0 to FF) in the **Hex** text box.
5. Click **Send**.
   The values of the lower eight digital output lines are output appropriately.

Testing Frequency Measurement

To verify that the module can perform a frequency measurement operation, do the following:

1. Wire an external clock source to counter/timer 0 on the DT9862 Series module. Refer to page 49 for an example of how to connect an external clock.

   Note: The Quick DataAcq application works only with counter/timer 0.

2. In the Quick DataAcq application, choose **Measure Frequency** from the **Acquisition** menu.
3. Select the appropriate DT9862 Series module from the **Board** list box.
4. In the **Count Duration** text box, enter the number of seconds during which events will be counted.
5. Click **Start** to start the frequency measurement operation.
   The operation automatically stops after the number of seconds you specified has elapsed, and the frequency is displayed on the screen.
6. Click **Stop** to stop the frequency measurement operation.

Testing Pulse Output

To verify that the module can perform a pulse output operation, perform the following steps:

1. Connect a scope to counter/timer 0 on the DT9862 Series module. Refer to page 52 for an example of how to connect a scope (a pulse output) to counter/timer 0.

   Note: The Quick DataAcq application works only with counter/timer 0.

2. In the Quick DataAcq application, choose **Pulse Generator** from the **Control** menu.
3. Select the appropriate DT9862 Series module from the **Board** list box.
4. Select either **Continuous** to output a continuous pulse stream or **One Shot** to output one pulse.
5. Select either **Low-to-high** to output a rising-edge pulse (the high portion of the total pulse output period is the active portion of the signal) or **High-to-low** to output a falling-edge pulse (the low portion of the total pulse output period is the active portion of the signal).
6. Under **Pulse Width**, enter a percentage or use the slider to select a percentage for the pulse width. The percentage determines the duty cycle of the pulse.
7. Click **Start** to generate the pulse(s).
   The application displays the results both in text and graphical form.
8. Click **Stop** to stop a continuous pulse output operation. One-shot pulse output operations stop automatically.

Part 2: Using Your Module

Principles of Operation

Figure 24 shows a block diagram of the DT9862 Series modules.

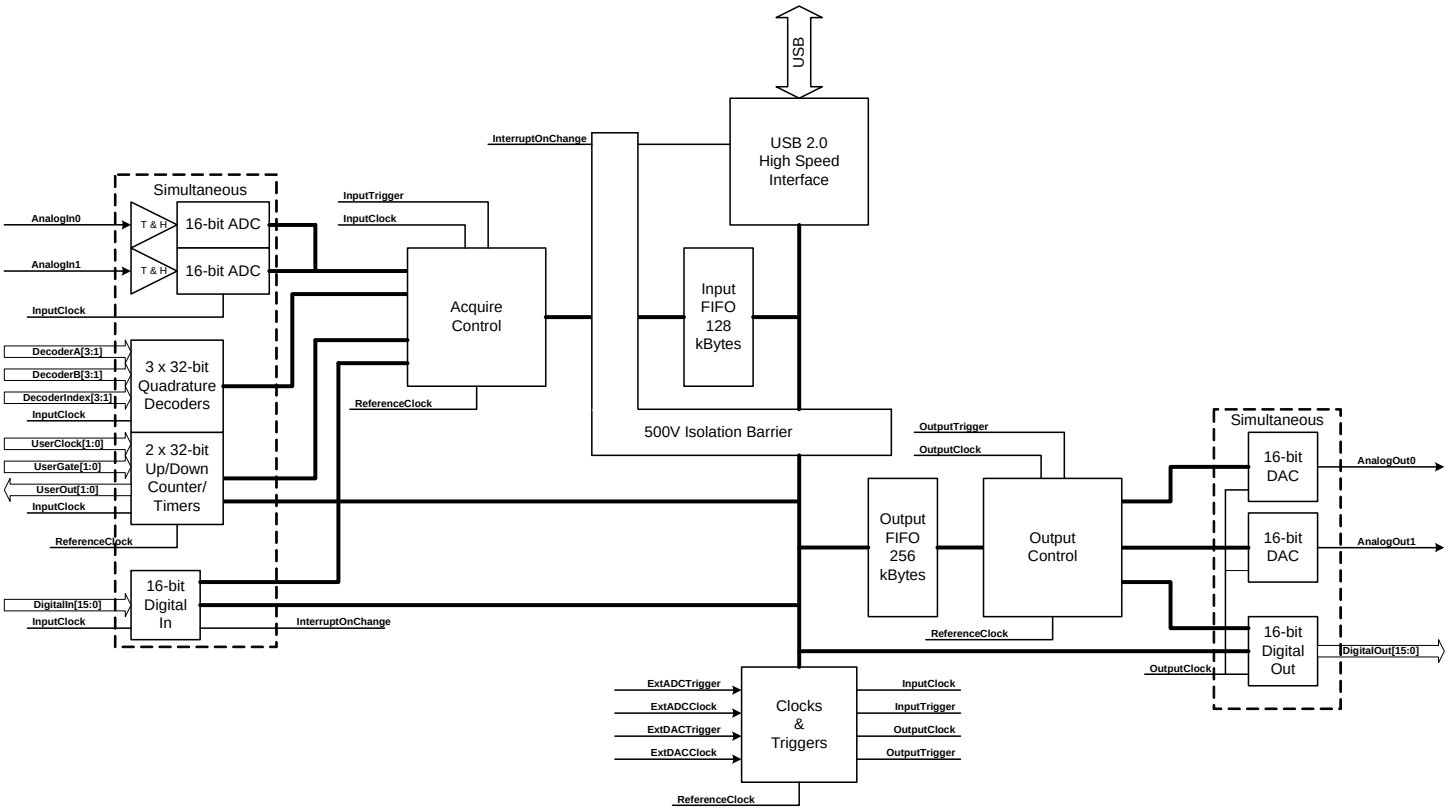


Figure 24: Block Diagram of the DT9862 Series Modules

Analog Input Features

This section describes the following features of analog input (A/D) operations on the DT9862 Series modules:

- Input resolution, described below
- Analog input channels, described below
- Input ranges, described on page 72
- Input sample clock sources, described on page 72
- Analog input conversion modes, described on page 74
- Input triggers, described on page 76
- Data format and transfer, described on page 77
- Error conditions, described on page 77

Input Resolution

Input resolution is fixed at 16 bits; you cannot specify the resolution in software.

Analog Input Channels

The DT9862 Series modules support two simultaneous analog inputs. You can connect the analog input channels in single-ended mode to the SMA connectors on the module. In this mode, the source of the input should be close to the module, and all the input signals are referred to the same common ground.

Note: To maintain simultaneous operation, all analog input connections must have the same lead lengths.

The DT9862 Series module can acquire data from a single analog input channel or from both analog input channels specified in a channel list. Channels are numbered 0 and 1.

The following subsections describe how to specify the channels.

Specifying a Single Analog Input Channel

The simplest way to acquire data from a single analog input channel is to specify the channel for a single-value analog input operation using software; refer to page 74 for more information about single-value operations.

You can also specify a single channel using the analog input channel list, described in the next section.

Specifying One or More Analog Input Channels

You can read data from one or more analog input channels using an analog input channel list. Because these modules feature simultaneous sampling, the order of the channels in the channel list does not matter. You cannot specify the same channel more than once in the list.

Using software, specify the channels that you want to sample. You can enter up to 13 entries in the channel list for the DT9862 Series module, including the analog input channels, digital input port, two 32-bit counter/timers, and three 32-bit quadrature decoders.

Channels 0 and 1 are reserved for analog input.

Specifying the Digital Input Port in the Analog Input Channel List

The DT9862 Series modules allow you to read the digital input port (all 16 digital input lines) using the analog input channel list. This feature is particularly useful when you want to correlate the timing of analog input and digital input events.

To read the digital input port, specify channel 2 in the analog input channel list. You can enter this channel anywhere in the list.

The digital input port is treated like any other channel in the analog input channel list; therefore, all the clocking, triggering, and conversion modes supported for analog input channels are supported for the digital input port, if you specify them this way.

Specifying Counter/Timers in the Analog Input Channel List

The DT9862 Series modules allow you to read the value of the 32-bit counter/timer channels using the analog input channel list. This feature is particularly useful when you want to correlate the timing of analog input and counter/timer events.

To read a counter/timer channel, specify the appropriate channel numbers in the analog input channel list (refer to Table 3 on page 71). You can enter the channel number anywhere in the list.

You need two channel list entries to read one 32-bit counter value. The first entry stores the lower 16-bit word, and the second entry stores the upper 16-bit word. You must specify both channel list entries, in sequential order, to include a counter/timer channel.

Table 3 lists the channel number(s) to use for each counter/timer.

Table 3: Using Counter/Timers in Analog Input Channel List

Counter/Timer Channel	Description	Channel to Specify in the Channel List
C/T_0_LOW	Lower 16 bits (0 to 15) of C/T 0	Channel 3
C/T_0_HI	Upper 16 bits (16 to 31) of C/T 0	Channel 4
C/T_1_LOW	Lower 16 bits (0 to 15) of C/T 1	Channel 5
C/T_1_HI	Upper 16 bits (16 to 31) of C/T 1	Channel 6

The counter/timer channel is treated like any other channel in the analog input channel list; therefore, all the clocking, triggering, and conversion modes supported for analog input channels are supported for the counter/timers, if you specify them this way.

Specifying Quadrature Decoders in the Analog Input Channel List

The DT9862 Series modules allow you to read the value of the 32-bit quadrature decoder channels using the analog input channel list. This feature is particularly useful when you want to correlate the timing of analog input measurements with rotational information.

To read a quadrature decoder channel, specify the appropriate channel numbers in the analog input channel list (refer to Table 4 on page 71). You can enter a channel number anywhere in the list.

You need two channel list entries to read one 32-bit counter value. The first entry stores the lower 16-bit word, and the second entry stores the upper 16-bit word. You must specify both channel list entries to include a quadrature decoder channel.

Table 4 lists the channel number(s) to use for each quadrature decoder.

Table 4: Using Quadrature Decoders in Analog Input Channel List

Quadrature Decoder Channel	Description	Channel to Specify in the Channel List
QUAD_0_LOW	Lower 16 bits of Q/D 0	Channel 7
QUAD_0_HI	Upper 16 bits of Q/D 0	Channel 8
QUAD_1_LOW	Lower 16 bits of Q/D 1	Channel 9
QUAD_1_HI	Upper 16 bits of Q/D 1	Channel 10
QUAD_2_LOW	Lower 16 bits of Q/D 2	Channel 11
QUAD_2_HI	Upper 16 bits of Q/D 2	Channel 12

Note: If you are using the DataAcq SDK, you access the quadrature decoders through the C/T subsystem. C/T subsystem 2 corresponds to quadrature decoder 0, C/T subsystem 3 corresponds to quadrature decoder 1, and C/T subsystem 4 corresponds to quadrature decoder 2.

The quadrature decoder channel is treated like any other channel in the analog input channel list; therefore, all the clocking, triggering, and conversion modes supported for analog input channels are supported for the quadrature decoders, if you specify them this way.

Input Ranges

The DT9862 module provides an input range of ±2.5 V. The DT9862S module provides an input range of ±1.25 V. Use software to specify the input range. Specify the gain as 1.

Input Sample Clock Sources

The DT9862 Series modules allow you to use one of the following clock sources to pace analog input operations:

- **Internal A/D clock** – Using software, specify the clock source as internal and the clock frequency at which to pace the operation.

  The DT9862 Series modules support a minimum sampling frequency of 500 kHz. The maximum sampling frequency depends on the number of channels and the types of channels included in the channel list.

  If you specify a number of samples to acquire that is less than or equal to the size of the 128 kByte input FIFO in continuous mode, you can acquire data at the maximum rate. This is know as a burst. For example, you can acquire data from both analog input channels at 10 MHz in burst mode. If you specify a number of samples to acquire that is greater than the size of the input FIFO, the DT9862 Series modules can achieve 10 MHz when sampling one analog input channel, 5 MHz when sampling two analog input channels, or 2 MHz or less when sampling other combination of input channels. Refer to Appendix E starting on page 155 for more information on the maximum throughput for various configurations of the channel list. Refer to page 74 for more information on continuous mode.

  When you specify the sampling frequency of the internal clock, the driver determines the actual frequency that the module can achieve by dividing the base clock frequency by an internal clock divider (an even value). It is possible that the actual sampling rate that is configured is different from the value that you specified. For example, assume that you requested a sampling frequency of 7 MHz. The base clock frequency is divided by the requested sampling frequency to determine the internal clock divider to use. In this example, 100 MHz / 7 MHz results in a clock divider of 14.29. Since only the integer portion of the clock divider is used, the actual sampling frequency is determined by dividing the base clock by the integer portion of the closest even clock divider (14 in this case). In this example, 100 MHz / 14 yields an actual sampling frequency of 7.142857 MHz; this is the frequency that the module uses.

- **External A/D clock** – An external A/D clock is useful when you want to pace acquisition at rates not available with the internal A/D clock.

  Connect an external A/D clock to the AD Clk connector on the DT9862 Series module. Conversions start on the falling edge of the external A/D clock input signal.

  Note: Ensure that you provide a clean, free running, clock signal with fast edges and a 50% duty cycle ±5%.

  Using software, specify the clock source as external. The clock frequency is always equal to the frequency of the external A/D sample clock input signal that you connect to the module.

Note: If you specify the digital input port and/or counter/timer or quadrature decoder channels in the channel list, the input sample clock (internal or external) also paces the acquisition of the digital input port and/or counter/timer and quadrature decoder channels.

Bandwidth of the DT9862

The DT9862 is a digitizer and provides a bandwidth of 10 MHz. It does not allow for under-sampling.

For the DT9862, specify a sampling frequency that is at least twice as fast as the input's highest frequency component (Nyquist sampling theory). For example, to accurately sample a 1 MHz signal, specify a sampling frequency of at least 2 MHz. Doing so avoids an error condition called *aliasing*, in which high frequency input components erroneously appear as lower frequencies after sampling.

Refer to Appendix F starting on page 159 for more information on the difference between digitizing and under-sampling.

Bandwidth of the DT9862S

The DT9862S is a sampler and provides a bandwidth of 300 MHz typical (100 MHz minimum), which allows under-sampling.

For example, if you know the approximate frequency of the signal that you are trying to acquire and the signal has a very stable frequency, you can use under-sampling to acquire many cycles of the waveform to recreate an accurate representation of the waveform.

Alternatively, you can use under-sampling to isolate and remove a known high frequency component from a signal.

Refer to Appendix F starting on page 159 for more information on under-sampling.

Analog Input Conversion Modes

The DT9862 Series modules support the following conversion modes:

- Single-value mode, described on page 74
- Continuous scan mode, described on page 74

Single-Value Mode

Single value operations are the simplest to use. Using software, you specify the analog input channel. The module acquires the data from the specified channel and returns the data immediately. For a single-value operation, you cannot specify a clock source, trigger source, scan mode, or buffer.

Single-value operations stop automatically when finished; you cannot stop a single-value operation.

Continuous Scan Mode

Continuous scan mode takes full advantage of the capabilities of a DT9862 Series module. Use continuous scan mode if you want to accurately control the period between successive simultaneous conversions of all channels in a channel list. You specify the channel list, clock source, trigger source, scan mode, and buffer using software.

When it detects an initial trigger, the module simultaneously samples all of the input channels, including the digital inputs, counter/timers, and quadrature decoders, and converts the data from the analog input channels. If the channel is included in the channel list, the sampled data is placed in the allocated buffer(s) and the operation continues until the allocated buffers are filled or until you stop the operation. Refer to page 77 for more information about buffers.

The conversion rate is determined by the frequency of the input sample clock; refer to page 72 for more information about the input sample clock. The sample rate, which is the rate at which a single entry in the channel list is sampled, is the same as the conversion rate due to the simultaneous nature of the module.

To select continuous scan mode, use software to specify the data flow as Continuous and to specify the initial trigger (the trigger source that starts the operation). You can select a software trigger, an external, positive digital (TTL) trigger, an external, negative digital (TTL) trigger, or a positive analog threshold trigger as the initial trigger. Refer to page 76 for more information about the supported trigger sources.

Figure 25 illustrates continuous scan mode using a channel list with three entries: channel 0, channel 1, and channel 2 (the digital input port). In this example, analog input data is acquired simultaneously on all channels on each clock pulse of the input sample clock. Data is acquired continuously.

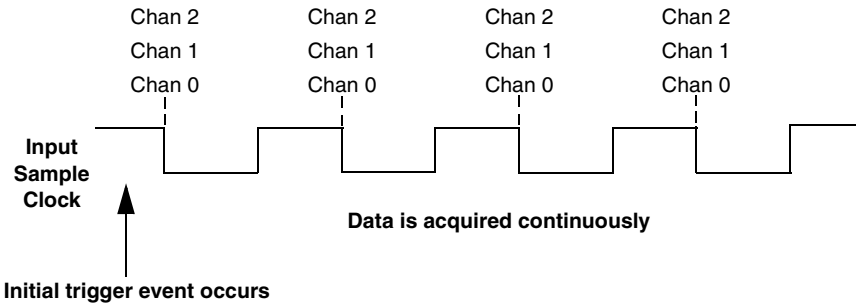


Figure 25: Continuous Scan Mode

Using software, you can stop a continuous scan by performing either an orderly stop or an abrupt stop. In an orderly stop, the module finishes acquiring the current buffer, stops all subsequent acquisition, and transfers the acquired data to host memory; any subsequent triggers are ignored.

In an abrupt stop, the module stops acquiring samples immediately; the current buffer is not completely filled, it is returned to the application only partially filled, and any subsequent triggers are ignored.

Maximum Acquisition Time for Analog Input Channels

If you specify a number of samples to acquire that is less than or equal to the size of the 128 kByte input FIFO in continuous mode, you can acquire data at the maximum rate. This is know as a burst. For example, you can acquire data from both analog input channels at 10 MHz in burst mode. In this case, the maximum acquire time for two analog input channels is 6.5536 ms, or 65536 samples per channel. This is determined as follows:

Number of bytes in buffer / (Sample freq x # bytes per chan x # of chans) = Total milliseconds

In this example:

(128 x 1024 bytes) / (10 MHz x 2 bytes per chan x 2 chan) = 3.2768 ms

3.2768 ms per channel x 10 MSamples/s =32768 samples/channel

If you specify a number of samples to acquire that is greater than the size of the input FIFO, the DT9862 Series can achieve 10 MHz when sampling one analog input channel, 5 MHz when sampling two analog input channels, or 2 MHz or less when sampling other combination of input channels. Refer to Appendix E starting on page 155 for more information on the maximum throughput for various configurations of the channel list. Refer to page 72 for more information on specifying the clock frequency.

Maximum Acquisition Time for Digital Input, Counter Timer, and Quadrature Decoder Channels

If your channel list contains anything other than analog input channels, the maximum sample rate is 2.5 MHz. Refer to Appendix E starting on page 155 for more information on the maximum throughput for various configurations of the channel list.

Digital input channels require 2 bytes/sample. Counter/timer and quadrature decoder channels require 4 bytes per sample.

For example, assume that the desired sample rate is 2 MHz and you want to acquire data from the digital input channel, both counters, and all three quadrature decoders when using a buffer size of 128 kBytes. In this case, the maximum acquire time for these channels is 2.9789 ms, or 5957 samples per channel. This is determined as follows:

(128 x 1024 bytes) / [(2 MSamples/s x 2 bytes/DIN sample x 1) + (2 MSamples/s x 4 bytes/CTR sample x 2) + (2MSamples/s x 4 bytes/Quad sample x 3)] = 2.9789 ms

2.9789 ms x 2 MSamples/ch = 5957 samples/ch

Input Triggers

A trigger is an event that occurs based on a specified set of conditions. Acquisition starts when the module detects the initial trigger event and stops when all the allocated buffers have been filled or when you stop the operation.

The DT9862 Series module supports the following trigger sources:

- **Software trigger** – A software trigger event occurs when you start the analog input operation (the computer issues a write to the module to begin conversions). Using software, specify the trigger source as a software trigger.
- **External digital (TTL) trigger** – An external digital (TTL) trigger event occurs when the DT9862 Series module detects either a rising-edge (positive) or falling-edge (negative) transition on the signal connected to the AD Trig connector on the module. Using software, specify the trigger source as an external, positive digital (TTL) trigger or an external, negative digital (TTL) trigger.
- **Analog threshold trigger** – An analog threshold trigger event occurs when the signal attached to analog input channel 0 rises above a user-specified threshold value. Using software, specify the trigger source as a positive threshold trigger, the threshold trigger channel as channel 0, and the threshold level as a value between 0 V and +2.5 V for the DT9862 or 0 to +1.25 V for the DT9862S. Hysteresis is fixed at 50 mV.

Data Format and Transfer

The DT9862 Series module uses offset binary data encoding, where 0000 represents negative full-scale and FFFFh represents positive full-scale. Use software to specify the data encoding as binary. The ADC outputs FFFFh for above-range signals, and 0000 for below-range signals.

Before you begin acquiring data, you must allocate buffers to hold the data. An event is raised whenever a buffer is filled. This allows you to move and/or process the data as needed.

Note: We recommend that you allocate a minimum of two buffers that can contain even multiples of 256 samples. In addition, it is recommended that the minimum buffer size is no less than 64K (66536) samples.

If you specify a number of samples to acquire that is less than or equal to the size of the 128 kByte input FIFO in continuous mode, you can acquire data at the maximum rate. This is called a burst. For example, you can acquire data from both analog input channels at 10 MHz in burst mode. If you specify a number of samples to acquire that is greater than the size of the input FIFO, the DT9862 Series can achieve 10 MHz when sampling one analog input channel, 5 MHz when sampling two analog input channels, or 2 MHz or less when sampling other combination of input channels. Refer to Appendix E starting on page 155 for more information on the maximum throughput for various configurations of the channel list. Refer to page 74 for more information on continuous mode.

Data is written to multiple allocated input buffers continuously; when no more empty buffers are available, the operation stops. The data is gap-free.

Error Conditions

The DT9862 Series modules can detect the following errors:

- Input over sample – Indicates that the input sample clock rate is too fast. This error is reported if a new sample clock occurs while the ADC is busy performing a conversion from the previous input sample clock.
- Input FIFO overflow – Indicates that the input data is not being transferred fast enough from the input FIFO on the module through the USB interface to the host. This error is reported if the input FIFO is full.

If one of these error conditions occurs, the module stops acquiring and transferring data to the host computer, and the driver reports a buffer overrun error.

To avoid this error, try one or more of the following:

- Reduce the clock rate of the A/D
- Increase the size of the buffers
- Increase the number of buffers
- Close any other applications that are running

- Run the program on a faster computer

Analog Output Features

This section describes the following features of analog output operations:

- Output resolution, described below
- Analog output channels, described below
- Output ranges and gains, described on page 80
- Output triggers, described on page 80
- Output clocks, described on page 81
- Data format and transfer, described on page 84
- Error conditions, described on page 84

Output Resolution

Input resolution is fixed at 16 bits; you cannot specify the resolution in software.

Analog Output Channels

The DT9862 Series modules support two DC-level analog output channels. Channels are numbered 0 and 1.

Note: An extra analog output (D/A) subsystem is provided on the DT9862 Series modules for controlling the analog threshold trigger. The threshold trigger DAC is the highest-numbered D/A subsystem supported by your module. Refer to page 76 for more information on analog threshold triggering.

The DACs are deglitched to prevent noise from interfering with the output signal. They power up to a value of 0 V ±10 mV. Unplugging the module resets the DACs to 0 V.

The DT9862 Series modules can output data to a single DAC or sequentially to both DACs and/or the digital output port. The following subsections describe how to specify the DACs/port.

Specifying a Single Analog Output Channel

The simplest way to output data to a single analog output channel is to specify the channel for a single-value analog output operation using software; refer to page 81 for more information about single-value operations.

You can also specify a single analog output channel using the output channel list, described in the next section.

Specifying Multiple Analog Output Channels and/or the Digital Output Port

You can output data to one or more analog output channels and/or the digital output port using the output channel list. This feature is particularly useful when you want to correlate the timing of analog and digital output events.

Using software, specify the data flow mode as Continuous for the D/A subsystem (described on page 81) and specify the output channels you want to update, where 0 is D/A Out Ch1, 1 is D/A Out Ch2, and 2 is the digital output port. You can enter a maximum of 3 entries in the output channel list and the channels must be in order.

Note that you can skip a channel in the list, however, if you do not want to update it. For example, if you want to update only DAC1 and the digital output port, specify channels 1 and 2 in the output channel list. If you want to update all the DACs and the digital output ports, specify channels 0, 1, and 2 in the output channel list. The channels are output in order from the first entry in the list to the last entry in the list.

Note: The digital output port is treated like any other channel in the output channel list; therefore, all the clocking, triggering, and conversion modes supported for analog output channels are supported for the digital output port, if you specify the digital output port in the output channel list.

Output Ranges and Gains

Each analog output channel on a DT9862 Series module can output bipolar analog output signals in the range of ±2.5 V. Specify the output range as ±2.5 V and the gain as 1.

Output Triggers

A trigger is an event that occurs based on a specified set of conditions. The DT9862 Series modules support the following output trigger sources:

- **Software trigger** – A software trigger event occurs when you start the analog output operation. Using software, specify the trigger source as a software trigger.
- **External digital (TTL) trigger** – An external digital (TTL) trigger event occurs when the DT9862 Series module detects a rising-edge or falling-edge transition on the signal connected to the DAC Trig connector on the module. Using software, specify the trigger source as either external, positive digital (TTL) trigger or external, negative digital (TTL) trigger.

Output Clocks

The DT9862 Series module allows you to use one of the following clock sources to pace analog output operations:

- **Internal DAC clock** – Using software, specify the clock source as internal and the clock frequency at which to pace the operation. The minimum frequency supported is 0.01164 Samples/s; the maximum frequency supported is 2 MSamples/s (with small steps < 100 mV) or 500 kHz (full-scale steps).

  When you specify the sampling frequency of the internal DAC clock, the driver determines the actual frequency that the module can achieve by dividing the base clock frequency by an internal clock divider. On the DT9862 Series, the base clock frequency for the analog output subsystem is 50 MHz and is derived from the analog input base clock frequency of 100 MHz for precise synchronization of the analog input and analog output subsystems. It is possible that the actual output frequency that is configured is different from the value that you specified. For example, assume that you requested a output frequency of 7.5 kHz. The base clock frequency is divided by the requested output frequency to determine the internal clock divider to use. In this example, 50 MHz / 7.5 kHz results in a clock divider of 6666.6666. Since only the integer portion of the clock divider is used, the actual output frequency is determined by dividing the base clock by the integer portion of the clock divider. In this example, 50 MHz / 6666 yields an actual output frequency of 7.50075 kHz; this is the frequency that the module uses.

- **External DAC clock** – An external DAC clock is useful when you want to pace conversions at rates not available with the output sample clock or when you want to pace at uneven intervals.

  Connect an external D/A clock to the DAC Clk connector on the DT9862 Series module. Analog output operations start on the rising edge of the external D/A clock signal.

  Using software, specify the clock source as external. The clock frequency is always equal to the frequency of the external D/A clock signal that you connect to the module.

Output Conversion Modes

The DT9862 Series modules support the following conversion modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. Use software to specify the analog output channel that you want to update, and the value to output from that channel. For a single-value operation, you cannot specify a clock source, trigger source, or buffer. Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Continuous analog output operations** take full advantage of the capabilities of the DT9862 Series modules. In this mode, you can specify an output channel list, clock source, trigger source, buffer, and buffer wrap mode. Two continuous analog output modes are supported: streaming and waveform generation mode. These modes are described in the following subsections.

Streaming Analog Output

Use streaming analog output mode if you want to accurately control the period between conversions of individual channels in the output channel list (refer to page 80 for information on specifying the output channel list).

Use software to fill the output buffer with the values that you want to write to the DACs and to the digital output port, if applicable. For example, if your output channel list contains only analog output channel 0 and the digital output port, specify the values in the output buffer as follows: the first output value for analog output channel 0, the first output value for the digital output port, the second output value for analog output channel 0, the second output value for the digital output port, and so on.

Note: If a signal is connected to analog output channel 1 in the above example, analog output channel 1 continuously outputs the last value that was written to it.

When it detects a trigger, the module starts writing the values from the output buffer to the channels specified in the output channel list. The operation repeats continuously until all the data is output from the buffers.

Make sure that the host computer transfers data to the output channel list fast enough so that the list does not empty completely; otherwise, an underrun error results.

To select streaming analog output mode, use software to specify the following parameters:

- Set the data flow as Continuous.
- Set WrapSingleBuffer to False to use multiple buffers (a minimum of two buffers is recommended).
- Set the trigger source to any of the supported trigger sources (refer to page 80).
- Set the clock source to any of the supported output clock sources (refer to page 81).

To stop a streaming analog output operation, you can stop sending data to the module, letting the module stop when it runs out of data, or you can perform either an orderly stop or an abrupt stop using software. In an orderly stop, the module finishes outputting the current buffer, and then stops; all subsequent triggers are ignored. In an abrupt stop, the module stops outputting samples immediately; all subsequent triggers are ignored.

Waveform Generation

Use waveform generation mode if you want to output a waveform repetitively.

Note: The waveform pattern size must be the same for all output channels, and the total number of samples must be a multiple of the total number of output channels.

Use software to fill the output buffer with the values that you want to write to the channels in the output channel list. For example, if your output channel list contains only analog output channel 0 and the digital output port, specify the values in the output buffer as follows: the first output value for analog output channel 0, the first output value for the digital output port, the second output value for analog output channel 0, the second output value for the digital output port, and so on.

For guaranteed operation with no overrun errors, use a waveform pattern that ranges from 2 to 131,072 samples (128 kSamples) if you are using one channel, 2 to 65,536 samples (64 kSamples) if you are using two channels, or 2 to 43,690 samples if you are using three channels.

Note: If more than one output channel is enabled, the pattern size must be the same for all output channels.

When it detects a trigger, the host computer transfers the entire waveform pattern to the module, and the module starts writing output values to the output channels, as determined by the output channel list. A single buffer is output repeatedly. Use software to allocate the memory and specify the waveform pattern.

To select waveform generation mode, use software to specify the following parameters:

- Set the data flow to Continuous.
- Set WrapSingleBuffer to True to use a single buffer. Refer to the following section for more information on this buffer wrap mode.
- Set the trigger source as any of the supported trigger sources (refer to page 80).
- Set the clock source to any of the supported output clock sources (refer to page 81).

Data Format and Transfer

Data from the host computer must use offset binary data encoding for analog output signals, where 0000 represents –2.5 V, and FFFFh represents +2.5 V. Using software, specify the data encoding as binary.

Before you begin writing data to the output channels, you must allocate and fill buffers with the appropriate data. An event is returned whenever a buffer is transferred to the module. This allows you to reuse that buffer, and refill it with additional output data.

Note: If WrapSingleBuffer is False, we recommend that you allocate a minimum of two buffers. If WrapSingleBuffer is True, we recommend that you allocate a minimum of one buffer.

In streaming mode, data is written from multiple output buffers continuously; when no more buffers of data are available, the operation stops. The data is gap-free. If the size of your buffers is less than 128 kSamples and you stop the analog output operation, the operation stops after the current buffer and the next buffer have been output.

If a single buffer is used (WrapSingleBuffer is True), data is written from a single output buffer continuously; when all the data in the buffer has been output, the module returns to the first location of the buffer and continues outputting the data. This process continues indefinitely until you stop it.

Note: If a single buffer is used and the allocated output buffer is equal to or less than the size of the output FIFO on the module (256 kBytes or 128 kSamples), the data is written once to the module. The module recycles the data, allowing you to output the same pattern continuously without any further CPU or USB bus activity.

Error Conditions

The DT9862 Series modules can detect the following errors:

- Output FIFO underflow – Indicates that the output FIFO data was not sent fast enough from the host to the module. This error is reported if an output sample clock occurs when a write to the output FIFO is initiated and the output FIFO is empty.

  If a write to the output FIFO is not initiated when the output FIFO is empty, it is assumed that the host has no more data to convert; the last values that were placed in the output FIFO are output continuously by the analog output channels and/or the digital output lines.

- DAC over sample – Indicates that the output sample clock rate is too fast. This error is reported if a new output sample clock occurs while the module is busy loading the next values from the output FIFO into the analog output channels and/or digital output preload registers.

If one of these error conditions occurs, the module stops outputting data to the host computer, and the driver reports a buffer underrun error.

To avoid this error, try one or more of the following:

- Reduce the clock rate of the analog output subsystem
- Increase the size of the buffers
- Increase the number of buffers
- Close any other applications that are running
- Run the program on a faster computer

Digital I/O Features

This section describes the following features of digital I/O operations:

- Digital I/O lines, described below
- Operation modes, described on page 86

Digital I/O Lines

The DT9862 Series modules support one digital input port, consisting of 16 digital input lines (lines 0 to 15) and one digital output port, consisting of 16 digital output lines (lines 0 to 15). The resolution is fixed at 16 bits; you cannot change the resolution in software.

You can read all 16 digital input lines or write all 16 digital output lines with a single-value digital I/O operation.

In addition, you can specify the digital input port in an analog input channel list to perform a continuous digital input operation, or you can specify the digital output port in an output channel list to perform a continuous digital output operation.

A digital line is high if its value is 1; a digital line is low if its value is 0. On power up or reset, a low value (0) is output from each of the digital output lines.

The DT9862 Series modules allow you to program the first eight digital input lines to perform interrupt-on-change operations. Refer to the next section for more information.

Operation Modes

The DT9862 Series modules support the following digital I/O operation modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. You use software to specify the digital I/O port (the gain is ignored). Data is then read from or written to all the digital I/O lines. For a single-value operation, you cannot specify a clock or trigger source.

  Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Continuous digital I/O** takes full advantage of the capabilities of the DT9862 Series modules using the analog I/O clock source, scan mode, trigger source, buffer, and buffer wrap mode.

  – ***Digital input*** – For digital input operations, enter the digital input port (all 16 digital input lines) as channel 2 in the analog input channel list; refer to page 70 for more information. The analog input sample clock (internal or external) paces the reading of the digital input port (as well as the acquisition of the analog input, counter/timer, and quadrature decoder channels); refer to page 72 for more information.

- ***Digital output*** – For digital output operations, enter the digital output port (all 16 digital output lines) as channel 2 in the output channel list; refer to page 80 for more information. The analog output clock (internal or external) paces the update of the digital output port (as well as the update of the analog output channels); refer to page 81 for more information.

- **Interrupt-on-change operations** – You can use the Open Layers Control Panel applet or the DT-Open Layers for .NET Class Library to select any of the first eight digital input lines to perform interrupt-on-change operations; refer to page 33 for more information.

  Use software to set the data flow mode of the digital I/O subsystem to Continuous. When any one of the specified bits changes state, the module reads the entire 16-bit digital input value and generates an interrupt. The software returns the current value of the digital input port as well as the digital input lines that changed state.

Note: If you are using the DataAcq SDK to perform a continuous digital input operation, use the *lParam* parameter of the **olDaSetWndHandle** or **olDaSetNotificationProcedure** function to determine which digital input line changed state and the status of the digital input port when the interrupt occurred.

The low byte of the first word of *lParam* contains the state of the digital input subsystem, where bit 0 corresponds to digital input line 0 and bit 7 corresponds to digital input line 7.

The high byte of the first word of *lParam* contains the digital lines (bits) that changed state causing the interrupt to occur, where bit 8 corresponds to digital input line 0 and bit 15 corresponds to digital input line 7.

Counter/Timer Features

This section describes the following features of counter/timer (C/T) operations:

- C/T channels, described below
- C/T clock sources, described on page 89
- Gate types, described on page 89
- Pulse types and duty cycles, described on page 90
- C/T operation modes, described on page 90

C/T Channels

The DT9862 Series modules provide two 32-bit counter/timers (C/T subsystems 0 and 1) for general-purpose use.

Each general-purpose counter accepts a clock input signal and gate input signal and outputs a pulse (pulse output signal), as shown in Figure 26.

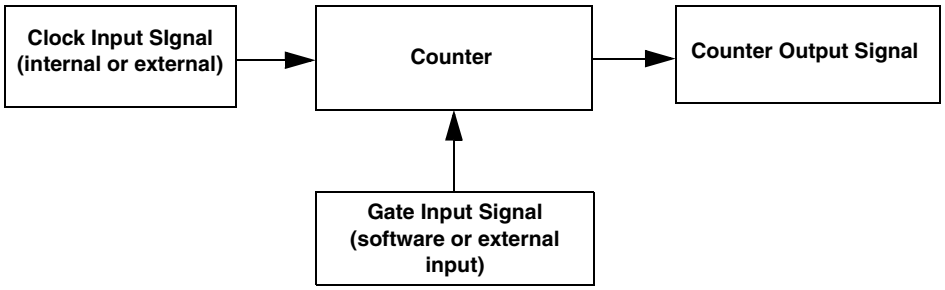


Figure 26: Counter/Timer Channel

To specify the counter/timer to use in software, specify the appropriate C/T subsystem.

Using software, you can also specify one or more of the counter/timers in the analog input channel list. You need two channel list entries to read a 32-bit counter value. The first entry stores the lower 16-bit word, and the second entry stores the upper 16-bit word. Refer to page 70 for more information about using C/Ts in the channel list.

C/T Clock Sources

The following clock sources are available for the general-purpose counter/timers:

- **Internal C/T clock** – Through software, specify the clock source as internal, and specify the frequency at which to pace the operation (this is the frequency of the Counter 0 Out or Counter 1 Out signal). This is typically used in rate generation mode.
- **External C/T clock** – An external C/T clock is useful when you want to pace counter/timer operations at rates not available with the internal C/T clock or if you want to pace at uneven intervals. The frequency of the external C/T clock can range up to 25 MHz.

  Connect the external clock to the Counter 0 Clock or Counter 1 Clock input signal on the DT9862 Series module. Counter/timer operations start on the rising edge of the clock input signal.

Note: You typically use the external C/T clock (the clock connected to the Counter 0 Clock or Counter 1 Clock input signal) to measure frequency (event counting), or to measure the time interval between edges (measure mode). The external C/T clock is not generally used for rate generation.

If you specify a counter/timer in the analog input channel list, the A/D clock determines how often you want to read the counter value. Refer to page 72 for more information about the A/D clock.

Gate Types

The edge or level of the Counter 0 Gate or Counter 1 Gate signal determines when a counter/timer operation is enabled. DT9862 Series modules provide the following gate types, which you can specify in software:

- **None** – A software command enables any counter/timer operation immediately after execution.
- **Logic-low level external gate input** – Enables a counter/timer operation when the counter gate signal is low, and disables the counter/timer operation when the counter gate signal is high. Note that this gate type is used for event counting and rate generation modes; refer to page 90 for more information about these modes.
- **Logic-high level external gate input** – Enables a counter/timer operation when the counter gate signal is high, and disables a counter/timer operation when the counter gate signal is low. Note that this gate type is used for event counting and rate generation modes; refer to page 90 for more information about these modes.
- **Falling-edge external gate input** – Enables a counter/timer operation when a high-to-low transition is detected on the counter gate signal. In software, this is called a low-edge gate type. Note that this gate type is used for edge-to-edge measurement, one-shot, and repetitive one-shot mode; refer to page 90 for more information about these modes.

- **Rising-edge external gate input** – Enables a counter/timer operation when a low-to-high transition is detected on the counter gate signal. In software, this is called a high-edge gate type. Note that this gate type is used for edge-to-edge measurement, one-shot, and repetitive one-shot mode; refer to page 90 for more information about these modes.

Pulse Output Types and Duty Cycles

The DT9862 Series modules can output the following types of pulses from each counter/timer:

- **High-to-low transitions** – The low portion of the total pulse output period is the active portion of the counter/timer clock output signal.
- **Low-to-high transitions** – The high portion of the total pulse output period is the active portion of the counter/timer pulse output signal.

You specify the pulse output type in software.

The duty cycle (or pulse width) indicates the percentage of the total pulse output period that is active. For example, a duty cycle of 50 indicates that half of the total pulse output is low and half of the total pulse output is high. You specify the duty cycle in software.

Figure 27 illustrates a low-to-high pulse with a duty cycle of approximately 30%.

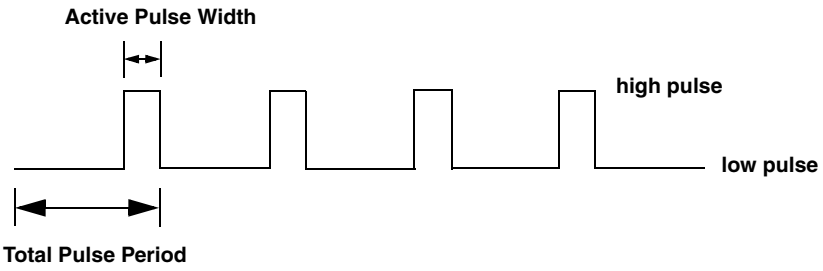


Figure 27: Example of a Low-to-High Pulse Output Type

Counter/Timer Operation Modes

The DT9862 Series modules support the following counter/timer operation modes:

- Event counting
- Up/down counting
- Frequency measurement
- Edge-to-edge measurement
- Continuous edge-to-edge measurement
- Rate generation
- One-shot

- Repetitive one-shot

Note: The active polarity for each counter/timer operation mode is software-selectable.

Event Counting

Use event counting mode if you want to count the number of rising edges that occur on the counter clock input when the counter gate signal is active (low-level or high-level). Refer to page 89 for information about specifying the active gate type.

You can count a maximum of 4,294,967,296 events before the counter rolls over to 0 and starts counting again.

Using software, specify the counter/timer mode as event counting (count), the C/T clock source as external, and the active gate type as low-level or high-level.

Make sure that the signals are wired appropriately. Refer to Chapter 3 for an example of connecting an event counting application.

Up/Down Counting

Use up/down counting mode if you want to increment or decrement the number of rising edges that occur on the counter clock input, depending on the level of the counter gate signal.

If the counter gate signal is high, the C/T increments; if the specified gate signal is low, the C/T decrements.

Using software, specify the counter/timer mode as up/down counting (up/down), and the C/T clock source as external. Note that you do not specify the gate type in software.

Make sure that the signals are wired appropriately. Refer to Chapter 3 for an example of connecting an up/down counting application.

Note: Initialize the counter/timer so that the C/T never increments above FFFFFFFFh or decrements below 0.

Frequency Measurement

Use frequency measurement mode if you want to measure the number of rising edges that occur on the counter clock input over a specified duration.

Using software, specify the counter/timer mode as frequency measurement (count) or event counting (count), the clock source as external, and the time over which to measure the frequency.

You can use the Windows timer (which uses a resolution of 1 ms), or if you need more accuracy than the Windows timer provides, you can connect a pulse of a known duration (such as a one-shot output of another user counter) to the counter gate input signal.

If you use a known pulse, use software to set up the counter/timers as follows:

1. Set up one of the counter/timers for one-shot mode, specifying the clock source as internal, the clock frequency, the gate type that enables the operation as rising edge or falling edge, and the polarity of the output pulse as high-to-low transition or low-to-high transition.
2. Set up the counter/timer that will measure the frequency for event counting mode, specifying the type of clock pulses to count and the gate type (this should match the pulse output type of the counter/timer set up for one-shot mode).
3. Start both counters (pulses are not counted until the active period of the one-shot pulse is generated).
4. Read the number of pulses counted. (Allow enough time to ensure that the active period of the one-shot occurred and that events have been counted.)
5. Determine the measurement period using the following equation:

$$\text{Measurement period} = \frac{1}{\text{Clock Frequency}} * \text{Active Pulse Width}$$

6. Determine the frequency of the clock input signal using the following equation:

$$\text{Frequency Measurement} = \frac{\text{Number of Events}}{\text{Measurement Period}}$$

Make sure that the signals are wired appropriately. One way to wire a frequency measurement operation is to use the same wiring as an event counting application, but not use an external gate signal. Refer to Chapter 3 for an example of connecting a frequency measurement application.

Edge-to-Edge Measurement

Use edge-to-edge measurement mode if you want to measure the time interval between a specified start edge and a specified stop edge.

The start edge and the stop edge can occur on the rising edge of the counter gate input, the falling edge of the counter gate input, the rising edge of the counter clock input, or the falling edge of the counter clock input. When the start edge is detected, the counter/timer starts incrementing, and continues incrementing until the stop edge is detected. The C/T then stops incrementing until it is enabled to start another measurement.

You can use edge-to-edge measurement mode to measure the following:

- Pulse width of a signal pulse (the amount of time that a signal pulse is in a high or a low state, or the amount of time between a rising edge and a falling edge or between a falling edge and a rising edge). You can calculate the pulse width as follows:
  - Pulse width = Number of counts/50 MHz

- Period of a signal pulse (the time between two occurrences of the same edge - rising edge to rising edge or falling edge to falling edge). You can calculate the period as follows:
  - Period = 1/Frequency
  - Period = Number of counts/50 MHz
- Frequency of a signal pulse (the number of periods per second). You can calculate the frequency as follows:
  - Frequency = 50 MHz/Number of Counts

When the operation completes, you can read the value of the counter.

Using software, specify the counter/timer mode as edge-to-edge measurement mode (measure), the C/T clock source as internal, the start edge type, and the stop edge type.

Make sure that the signals are wired appropriately. Refer to Chapter 3 for an example of connecting an edge-to-edge measurement application.

Continuous Edge-to-Edge Measurement

In continuous edge-to-edge measurement mode, the counter starts incrementing when it detects the specified start edge. When it detects the next start edge type, the value of the counter is stored and the next edge-to-edge measurement operation begins automatically.

Every time an edge-to-edge measurement operation completes, the previous measurement is overwritten with the new value. When you read the counter as part of the analog input data stream, the current value (from the last edge-to-edge measurement operation) is returned and the value of the counter is reset to 0. Refer to page 92 for more information on edge-to-edge measurement mode.

Note: If you read the counter before the measurement is complete, 0 is returned.

For example, you might see results similar to the following if you read the value of the counter/timer as part of the analog input data stream:

Table 5: An Example of Performing a Continuous Edge-to-Edge Measurement Operation as Part of the Analog Input Channel List

Time	A/D Value	Counter/Timer Value	Status of Continuous Edge-to-Edge Measurement Mode
10	5002	0	Operation started when the C/T subsystem was configured, but is not complete
20	5004	0	Operation not complete
30	5003	0	Operation not complete
40	5002	12373	Operation complete

Table 5: An Example of Performing a Continuous Edge-to-Edge Measurement Operation as Part of the Analog Input Channel List (cont.)

Time	A/D Value	Counter/Timer Value	Status of Continuous Edge-to-Edge Measurement Mode
50	5000	0	Next operation started, but is not complete
60	5002	0	Operation not complete
70	5004	0	Operation not complete
80	5003	12403	Operation complete
90	5002	0	Next operation started, but is not complete

To select continuous edge-to-edge measurement mode, use software to specify the counter/timer mode as continuous measure, the C/T clock source as internal, and the start edge type.

Rate Generation

Use rate generation mode to generate a continuous pulse output signal from the Counter 0 Out or Counter 1 Out line; this mode is sometimes referred to as continuous pulse output or pulse train output. You can use this pulse output signal as an external clock to pace other operations, such as analog input, analog output, or other counter/timer operations.

The pulse output operation is enabled whenever the counter gate signal is at the specified level. While the pulse output operation is enabled, the counter outputs a pulse of the specified type and frequency continuously. As soon as the operation is disabled, rate generation stops.

The period of the output pulse is determined by the C/T clock source (either internal using a clock divider, or external). You can output pulses using a maximum frequency of 25 MHz (this is the frequency of the counter output signal). Refer to page 89 for more information about the C/T clock sources.

Using software, specify the counter/timer mode as rate generation (rate), the C/T clock source as either internal or external, the clock divider (for an internal clock), the polarity of the output pulses (high-to-low transition or low-to-high transition), the duty cycle of the output pulses, and the active gate type (low-level or high-level). Refer to page 90 for more information about pulse output signals and to page 89 for more information about gate types.

Make sure that the signals are wired appropriately. Refer to Chapter 3 for an example of connecting a rate generation application.

One-Shot

Use one-shot mode to generate a single pulse output signal from the Counter 0 Out or Counter 1 Out line when the specified edge is detected on the counter gate signal. You can use this pulse output signal as an external digital (TTL) trigger to start other operations, such as analog input or analog output operations.

After the single pulse is output, the one-shot operation stops. All subsequent clock input signals and gate input signals are ignored.

The period of the output pulse is determined by the C/T clock source (either internal using a clock divider, or external). Note that in one-shot mode, the internal C/T clock is more useful than an external C/T clock; refer to page 89 for more information about the C/T clock sources.

Using software, specify the counter/timer mode as one-shot, the clock source as internal (recommended), the clock divider, the polarity of the output pulse (high-to-low transition or low-to-high transition), and the active gate type (rising edge or falling edge). Refer to page 90 for more information about pulse output types and to page 89 for more information about gate types.

Note: In the case of a one-shot operation, a duty cycle of 100% is set automatically.

Make sure that the signals are wired appropriately. Refer to Chapter 3 for an example of connecting a one-shot application.

Repetitive One-Shot

Use repetitive one-shot mode to generate a pulse output signal from the Counter 0 Out or Counter 1 Out line whenever the specified edge is detected on the counter gate signal. You can use this mode to clean up a poor clock input signal by changing its pulse width, and then outputting it.

The module continues to output pulses until you stop the operation. Note that any counter gate signals that occur while the pulse is being output are not detected by the module.

The period of the output pulse is determined by the C/T clock source (either internal using a clock divider, or external). Note that in repetitive one-shot mode, the internal C/T clock is more useful than an external clock; refer to page 89 for more information about the C/T clock sources.

Using software, specify the counter/timer mode as repetitive one-shot, the polarity of the output pulses (high-to-low transition or low-to-high transition), the C/T clock source as internal (recommended), and the active gate type (rising edge or falling edge). Refer to page 90 for more information about pulse output types and to page 89 for more information about gates.

Note: In the case of a one-shot operation, a duty cycle of 100% is set automatically.

Make sure that the signals are wired appropriately. Refer to Chapter 3 for an example of connecting a repetitive one-shot application.

Quadrature Decoder Features

The DT9862 Series modules provide three 32-bit quadrature decoders that allow simultaneous decoding of three quadrature encoded inputs. Quadrature decoders may be used to provide relative or absolute position, or determine rotational speed by calculating the difference between samples.

To specify the quadrature decoder to use in software, specify the appropriate QUAD subsystem. For example, quadrature decoder 0 corresponds to QUAD subsystem element 0, and quadrature decoder 1 corresponds to QUAD subsystem element 1.

Note: If you are using the DataAcq SDK, you access the quadrature decoders through the C/T subsystem. C/T subsystem 2 corresponds to quadrature decoder 0, C/T subsystem 3 corresponds to quadrature decoder 1, and C/T subsystem 4 corresponds to quadrature decoder 2.

Using software, you can also specify one or more of the quadrature decoders in the analog input channel list. You need two channel list entries to read a 32-bit quadrature decoder value. The first entry stores the lower 16-bit word, and the second entry stores the upper 16-bit word. Refer to page 71 for more information about using quadrature decoders in the channel list.

Each quadrature decoder supports "A," "B," and "Index" inputs and is used to interface with a quadrature encoder sensor. The A and B input relationships are used to increment or decrement the positional count; the Index input can be used to zero-out the positional count.

Figure 28 shows an example of a quadrature decoder mode. In this case, the A input leads the B input, up counting with a 90 degree Index.

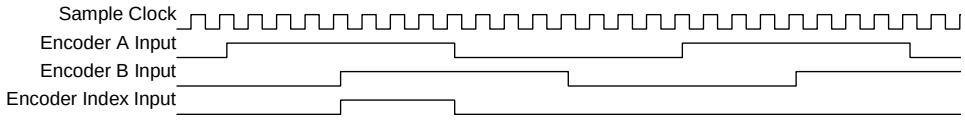


Figure 28: Example Quadrature Decoder Mode

Using software, you can specify the following parameters for a quadrature decoder operation:

- The pre-scale value that is used to filter the onboard clock. Using a pre-scale value can remove ringing edges and unwanted noise for more accurate data.
- The scaling mode (X1 or X4 mode), which determines the resolution of the quadrature encoder. In X1 mode, the quadrature decoder counts the edges on the A signal input. In X4, mode the quadrature decoder counts the edges on the A and B signal inputs.

  Therefore, if a quadrature decoder has 360 pulses per revolution, X1 mode yields 360 counts when the quadrature decoder is rotated 360 degrees. X4 mode yields four times the number of counts, or 1440 (360 x 4) when the quadrature decoder is rotated 360 degrees.

- The index mode, which either enables the Index signal or disables the Index signal. Note that if the scaling mode is X4, the index mode must be disabled.

Note: For quadrature decoder operations, set the clock source to external.

You can read the value of the quadrature decoder subsystem to determine relative or absolute position.

To determine the rotation of a quadrature encoder, use one of the following formulas:

X1 Scaling Mode:

$$\textit{Rotation degrees} = \frac{\textit{Count}}{N} \times 360 \text{ degrees}$$

where *N* is the number of pulses generated by the quadrature encoder per rotation. For example, assume that you are using X1 scaling mode. If every rotation of the quadrature encoder generated 10 pulses, and the value that is read from the quadrature decoder is 5, the rotation of the quadrature encoder is 180 degrees (5/10 x 360 degrees).

X4 Scaling Mode:

$$\textit{Rotation degrees} = \frac{\textit{Count}}{4 * N} \times 360 \text{ degrees}$$

where *N* is the number of pulses generated by the quadrature encoder per rotation. For example, assume that you are using X4 scaling mode. If every rotation of the quadrature encoder generated 10 pulses, and the value that is read from the quadrature decoder is 20, the rotation of the quadrature encoder is 180 degrees (20/40 x 360 degrees).

Supported Device Driver Capabilities

The DT9862 Series Device Driver provides support for the analog input (A/D), analog output (D/A), digital input (DIN), digital output (DOUT), counter/timer (C/T), and quadrature decoder (QUAD) subsystems. For information on how to configure the device driver, refer to page 33.

Table 6: DT9862 Series Subsystems

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Total Subsystems on Module	1	1 or 2[a]	1	1	2	0	3

a. If your module does not support analog output operations, element 0 of the D/A subsystem is used for the analog threshold trigger. If your module does support analog output operations, element 0 of the D/A subsystem contains the analog output channels, and element 1 of the D/A subsystem is used for the analog threshold trigger.

The tables in this chapter summarize the features available for use with the DT-Open Layers for .NET Class Library and the DT9862 Series module. The DT-Open Layers for .NET Class Library provides properties that return support information for specified subsystem capabilities.

The first row in each table lists the subsystem types. The first column in each table lists all possible subsystem capabilities. A description of each capability is followed by the property used to describe that capability in the DT-Open Layers for .NET Class Library.

Note: The following tables include the capabilities that can be queried. However, some capabilities may not be supported by your device. Blank fields represent unsupported options.

For more information, refer to the description of these properties in the DT-Open Layers for .NET Class Library online help or *DT-Open Layers for .NET Class Library User's Manual*.

Data Flow and Operation Options

Table 7: Data Flow and Operation Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Single-Value Operation Support **SupportsSingleValue**	Yes	Yes	Yes	Yes	Yes		Yes
Simultaneous Single-Value Output Operations **SupportsSetSingleValues**							
Continuous Operation Support **SupportsContinuous**	Yes	Yes	Yes[a]	Yes[b]	Yes[c]		Yes[d]
Continuous Operation until Trigger **SupportsContinuousPreTrigger**							
Continuous Operation before & after Trigger **SupportsContinuousPrePostTrigger**							
Waveform Operations Using FIFO Only **SupportsWaveformModeOnly**							
Simultaneous Start List Support **SupportsSimultaneousStart**	Yes	Yes					
Supports Programmable Synchronization Modes **SupportsSynchronization**							
Synchronization Modes **SynchronizationMode**							
Interrupt Support **SupportsInterruptOnChange**			Yes[e]				
FIFO Size **FifoSize**	128 kByte	256 kByte					
Muting and Unmuting the Output Voltage **SupportsMute**		Yes					
Auto-Calibrate Support **SupportsAutoCalibrate**							

a. The DIN subsystem supports continuous mode by allowing you to read the digital input port (all 16 digital input lines) using the analog input channel list.
b. The DOUT subsystem supports continuous mode by allowing you to output data from the digital output port (all 16 digital output lines) using the output channel list.
c. The C/T subsystem supports continuous mode by allowing you to read the value of one or more of the two general-purpose counter/timer channels using the analog input channel list.
d. The QUAD subsystem supports continuous mode by allowing you to read the value of one or more of the three quadrature decoders using the analog input channel list.
e. The first eight digital input lines of the digital input port can generate an interrupt-on-change event. You enable the interrupts on a line-by-line basis during driver configuration; refer to page 33 for more information on configuring the driver. If you are using the DataAcq SDK, refer to page 86 for more information about determining which digital input lines changed state.

Buffering

Table 8: Buffering Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Buffer Support **SupportsBuffering**	Yes	Yes					
Single Buffer Wrap Mode Support **SupportsWrapSingle**		Yes					
Inprocess Buffer Flush Support **SupportsInProcessFlush**	Yes[a]						

a. Data from DT9862 Series modules is transferred to the host in 4,096-byte (2,048-sample) segments. If the application moves data from the buffer before the module has transferred 2,048 samples to the host, the resulting buffer will contain 0 samples. Your application program must deal with these situations when flushing an inprocess buffer.

Triggered Scan Mode

Table 9: Triggered Scan Mode Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Triggered Scan Support **SupportsTriggeredScan**							
Maximum Number of CGL Scans per Trigger **MaxMultiScanCount**	1	0	0	0	0		0
Maximum Retrigger Frequency **MaxRetriggerFreq**	0	0	0	0	0		0
Minimum Retrigger Frequency **MinRetriggerFreq**	0	0	0	0	0		0

Data Encoding

Table 10: Data Encoding Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Binary Encoding Support **SupportsBinaryEncoding**	Yes	Yes	Yes	Yes	Yes		Yes
Twos Complement Support **SupportsTwosCompEncoding**							
Returns Floating-Point Values **ReturnsFloats**							

Channels

Table 11: Channel Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Number of Channels **NumberOfChannels**	13[a]	2[b]	1	1	2		3
SE Support **SupportsSingleEnded**	Yes						
SE Channels **MaxSingleEndedChannels**	2	0	0	0	0		0
DI Support **SupportsDifferential**		Yes	Yes	Yes	Yes		Yes
DI Channels **MaxDifferentialChannels**	0	2	1	1	2		3
Maximum Channel-Gain List Depth **CGLDepth**	13[a]	3[b]	0	0	0		0
Simultaneous Sample-and-Hold Support **SupportsSimultaneousSampleHold**	Yes						
Channel-List Inhibit **SupportsChannelListInhibit**							
Support MultiSensor Inputs **SupportsMultiSensor**							
Bias Return Termination Resistor Support **SupportsInputTermination**							

a. Analog input channels are numbered 0 and 1. You can read the digital input port by specifying channel 2 in the input channel list. You can read counter/timer 0 by specifying channels 3 and 4 in the input channel list. You can read counter/timer 1 by specifying channels 5 and 6 in the input channel list. You can read quadrature decoder 0 by specifying channels 7 and 8 in the input channel list. You can read quadrature decoder 1 by specifying channels 9 and 10 in the input channel list. You can read quadrature decoder 2 by specifying channels 11 and 12 in the input channel list.

b. Analog output channels are numbered 0 and 1. You can update the digital output port by specifying channel 2 in the output channel list.

Gain

Table 12: Gain Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Programmable Gain Support **SupportsProgrammableGain**	Yes						
Number of Gains **NumberOfSupportedGains**	1	1	1	1	0		0
Gains Available **SupportedGains**	1	1	1	1			

Ranges

Table 13: Range Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Number of Voltage Ranges **NumberOfRanges**	1	1	0	0	0		0
Available Ranges **SupportedVoltageRanges**	±2.5 V or ±1.25 V[a]	±2.5 V or 0 to 2.5 V[b]					

a. The DT9862 supports an input voltage range of ±2.5 V; the DT9862S supports an input voltage range of ±1.25 V.
b. For the D/A subsystem that contains the analog output channels, the output range is ±2.5 V. For the D/A subsystem that is used as the threshold trigger, the range is 0 to 2.5 V, where a raw count of 0 represents 0 V and a raw count of 255 represents 2.5 V.

Resolution

Table 14: Resolution Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Software Programmable Resolution **SupportsSoftwareResolution**							
Number of Resolutions **NumberOfResolutions**	1	1	1	1	1		1
Available Resolutions **SupportedResolutions**	16	16 or 8[a]	16	16	32		32

a. For the D/A subsystem that contains the analog output channels, the resolution is 16 bits. For the D/A subsystem that is used to set the analog threshold value, the resolution is 8 bits.

Current and Resistance Support

Table 15: Current and Resistance Support Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Current Support **SupportsCurrent**							
Current Output Support **SupportsCurrentOutput**							
Resistance Support **SupportsResistance**							
Software Programmable External Excitation Current Source for Resistance **SupportsExternalExcitationCurrentSrc**							
Software Programmable Internal Excitation Current Source **SupportsInternalExcitationCurrentSrc**							
Available Excitation Current Source Values **SupportedExcitationCurrentValues**							

Thermocouple, RTD, and Thermistor Support

Table 16: Thermocouple, RTD, and Thermistor Support Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Thermocouple Support **SupportsThernocouple**							
RTD Support **SupportsRTD**							
Thermistor Support **SupportsThermistor**							
Voltage Converted to Temperature **SupportsTemperatureDataInStream**							
Supported Thermocouple Types **ThermocoupleType**							
Supports CJC Source Internally in Hardware **SupportsCjcSourceInternal**							
Supports CJC Channel **SupportsCjcSourceChannel**							
Available CJC Channels **CjcChannel**							
Supports Interleaved CJC Values in Data Stream **SupportsInterleavedCjcTemperaturesInStream**							
Supported RTD Types **RTDType**							
RTD R0 Coefficient **RtdR0**							
Supports Temperature Filters **SupportsTemperatureFilters**							
Programmable Filter Types **TemperatureFilterType**							

IEPE Support

Table 17: IEPE Support Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
IEPE SupportS **SupportsIEPE**							
Software Programmable AC Coupling **SupportsACCoupling**							
Software Programmable DC Coupling **SupportsDCCoupling**							
Software Programmable External Excitation Current Source **SupportsExternalExcitationCurrentSrc**							
Software Programmable Internal Excitation Current Source **SupportsInternalExcitationCurrentSrc**							
Available Excitation Current Source Values **SupportedExcitationCurrentValues**							

Bridge and Strain Gage Support

Table 18: Bridge and Strain Gage Support Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Bridge Support **SupportsBridge**							
Supported Bridge Configurations **BridgeConfiguration**							
Strain Gage Support **SupportsStrainGage**							
Supported Strain Gage Bridge Configurations **StrainGageBridgeConfiguration**							
External Excitation Voltage **SupportsExternalExcitationVoltage**							
Internal Excitation Voltage **SupportsInternalExcitationVoltage**							
Shunt Calibration **SupportsShuntCalibration**							
Voltage Excitation Per Channel **SupportedPerChannelVoltageExcitation**							
Minimum Excitation Voltage **MinExcitationVoltage**							
Maximum Excitation Voltage **MaxExcitationVoltage**							

Start Triggers

Table 19: Trigger Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Software Trigger Support **SupportsSoftwareTrigger**	Yes	Yes	Yes	Yes	Yes		Yes
External Positive TTL Trigger Support **SupportsPosExternalTTLTrigger**	Yes	Yes			Yes		Yes
External Negative TTL Trigger Support **SupportsNegExternalTTLTrigger**	Yes	Yes					
External Positive TTL Trigger Support for Single-Value Operations **SupportsSvPosExternalTTLTrigger**							
External Negative TTL Trigger Support for Single-Value Operations **SupportsSvNegExternalTTLTrigger**							
Positive Threshold Trigger Support **SupportsPosThresholdTrigger**	Yes[a]						
Negative Threshold Trigger Support **SupportsNegThresholdTrigger**							
Digital Event Trigger Support **SupportsDigitalEventTrigger**							
Threshold Trigger Channel **SupportedThresholdTriggerChannel**	0						
Post-Trigger Scan Countl **SupportsPostTriggerScanCount**							

a. Using software, specify a threshold value between 0 V and +2.5 V for the DT9862 or 0 V and +1.25 V for the DT9862S, and specify the threshold channel as analog input channel 0.

Reference Triggers

Table 20: Reference Trigger Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
External Positive TTL Trigger Support **SupportsPosExternalTTLTrigger**							
External Negative TTL Trigger Support **SupportsNegExternalTTLTrigger**							
Positive Threshold Trigger Support **SupportsPosThresholdTrigger**							
Negative Threshold Trigger Support **SupportsNegThresholdTrigger**							
Digital Event Trigger Support **SupportsDigitalEventTrigger**							
Sync Bus Support **SupportsSyncBusTrigger**							
Analog Input Channels Supported for the Threshold Trigger **SupportedThresholdTriggerChannels**							
Post-Trigger Scan Count Support **SupportsPostTriggerScanCount**							

Clocks

Table 21: DT9862 Series Clock Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	QUAD
Internal Clock Support **SupportsInternalClock**	Yes	Yes	Yes	Yes		
External Clock Support **SupportsExternalClock**	Yes	Yes			Yes	Yes
Simultaneous Input/Output on a Single Clock Signal **SupportsSimultaneousClocking**	Yes	Yes				
Base Clock Frequency **BaseClockFrequency**	100 MHz[a]	50 MHz[b]	0	0	50 MHz	50 MHz
Maximum Clock Divider **MaxExtClockDivider**	0	0	1	1	2147483648	2147483648
Minimum Clock Divider **MinExtClockDivider**	0	0	1	1	2	2
Maximum Frequency **MaxFrequency**	10 MHz	2 MHz	0	0	25 MHz	25 MHz
Minimum Frequency **MinFrequency**	500 kHz	0.01164 Hz	0	0	0.02328 Hz	0.02328 Hz

a. The driver determines the actual sampling frequency by dividing the base clock frequency by an internal clock divider (an even value)

b. The driver determines the actual sampling frequency by dividing the base clock frequency by the internal clock divider.

Counter/Timers

Table 22: DT9862 Series Counter/Timer Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	QUAD
Cascading Support **SupportsCascading**						
Event Count Mode Support **SupportsCount**					Yes	
Generate Rate Mode Support **SupportsRateGenerate**					Yes	
One-Shot Mode Support **SupportsOneShot**					Yes	
Repetitive One-Shot Mode Support **SupportsOneShotRepeat**					Yes	
Up/Down Counting Mode Support **SupportsUpDown**					Yes	
Edge-to-Edge Measurement Mode Support **SupportsMeasure**					Yes	
Continuous Edge-to-Edge Measurement Mode Support **SupportsContinuousMeasure**					Yes	
High to Low Output Pulse Support **SupportsHighToLowPulse**					Yes	
Low to High Output Pulse Support **SupportsLowToHighPulse**					Yes	
Variable Pulse Width Support **SupportsVariablePulseWidth**					Yes[a]	
None (internal) Gate Type Support **SupportsGateNone**					Yes	
High Level Gate Type Support **SupportsGateHighLevel**					Yes[b]	
Low Level Gate Type Support **SupportsGateLowLevel**					Yes[b]	
High Edge Gate Type Support **SupportsGateHighEdge**					Yes[b]	
Low Edge Gate Type Support **SupportsGateLowEdge**					Yes[b]	
Level Change Gate Type Support **SupportsGateLevel**						
Clock-Falling Edge Type **SupportsClockFalling**					Yes	
Clock-Rising Edge Type **SupportsClockRising**					Yes	
Gate-Falling Edge Type **SupportsGateFalling**					Yes	

Table 22: DT9862 Series Counter/Timer Options (cont.)

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	QUAD
Gate-Rising Edge Type **SupportsGateRising**					Yes	
Interrupt-Driven Operations **SupportsInterrupt**						

a. In one-shot and repetitve one-shot mode, the pulse width is set to 100% automatically.
b. High-edge and low-edge are supported for one-shot and repetitive one-shot modes. High-level and low-level are supported for event counting, up/down counting, frequency measurement, edge-to-edge measurement, continuous edge-to-edge measurement, and rate generation modes.

Tachometers

Table 23: Tachometer Options

DT9862 Series	A/D	D/A	DIN	DOUT	C/T	TACH	QUAD
Tachometer Falling Edges **SupportsFallingEdge**							
Tachometer Rising Edges **SupportsRisingEdge**							
Tachometer Stale Data Flag **SupportsStaleDataFlag**							

7

Troubleshooting

General Checklist

Should you experience problems using a DT9862 Series module, do the following:

1. Read all the documentation provided for your product, including any "Read This First" information.
2. Check the OMNI CD for any README files and ensure that you have used the latest installation and configuration information available.
3. Check that your system meets the requirements stated on page 28.
4. Check that you have installed your hardware properly using the instructions in Chapter 2.
5. Check that you have installed and configured the device driver properly using the instructions in Chapter 2.
6. Check that you have wired your signals properly using the instructions in Chapter 3.
7. Search the DT Knowledgebase in the Support section of the Data Translation web site (at www.datatranslation.com) for an answer to your problem.
8. Visit the product's page on the Data Translation web site for the latest tips, white papers, product documentation, and software fixes.

If you still experience problems, try using the information in Table 24 to isolate and solve the problem. If you cannot identify the problem, refer to page 116.

Table 24: Troubleshooting Problems

Symptom	Possible Cause	Possible Solution
Module is not recognized.	You plugged the module into your computer before installing the device driver.	From the Control Panel > System > Hardware > Device Manager, uninstall any unknown devices (showing a yellow question mark). Then, run the setup program on your OMNI CD to install the USB device drivers, and reconnect your USB module to the computer.
Module does not respond.	The module configuration is incorrect.	Check the configuration of your device driver; see the instructions in Chapter 2.
	The module is damaged.	Contact Data Translation for technical support; refer to page 116.
Intermittent operation.	Loose connections or vibrations exist.	Check your wiring and tighten any loose connections or cushion vibration sources; see the instructions in Chapter 3.
	The module is overheating.	Check environmental and ambient temperature; consult the module's specifications on page 134 of this manual and the documentation provided by your computer manufacturer for more information.
	Electrical noise exists.	Check your wiring and either provide better shielding or reroute unshielded wiring; see the instructions in Chapter 3.

Table 24: Troubleshooting Problems (cont.)

Symptom	Possible Cause	Possible Solution
Device failure error reported.	The DT9862 Series module cannot communicate with the Microsoft bus driver or a problem with the bus driver exists.	Check your cabling and wiring and tighten any loose connections; see the instructions in Chapter 3.
	The DT9862 Series module was removed while an operation was being performed.	Ensure that your DT9862 Series module is properly connected; see the instructions in Chapter 2.
Data appears to be invalid.	An open connection exists.	Check your wiring and fix any open connections; see the instructions in Chapter 3.
	A transducer is not connected to the channel being read.	Check the transducer connections; see the instructions in Chapter 3.
	The module is set up for differential inputs while the transducers are wired as single-ended inputs or vice versa.	Check your wiring and ensure that what you specify in software matches your hardware configuration; see the instructions in Chapter 3.
	The DT9862 Series module is out of calibration.	DT9862 Series modules are calibrated at the factory. If you want to readjust the calibration of the analog input or analog output circuitry, refer to Chapter 8 starting on page 119.
	The cable impedance is not matched at the source.	Ensure proper cable matching, as discussed on page 37.
USB 2.0 is not recognized.	Your operating system does not have the appropriate Service Pack installed.	Ensure that you load the appropriate Windows Service Pack. If you are unsure of whether you are using USB 2.0 or USB 1.1, run the Open Layers Control Panel applet, described in Chapter 2.
	Standby mode is enabled on your PC.	For some PCs, you may need to disable standby mode on your system for proper USB 2.0 operation. Consult Microsoft for more information.

Technical Support

If you have difficulty using a DT9862 Series module, Data Translation's Technical Support Department is available to provide technical assistance.

To request technical support, go to our web site at http://www.datatranslation.com and click on the Support link.

When requesting technical support, be prepared to provide the following information:

- Your product serial number
- The hardware/software product you need help on
- The version of the OMNI CD you are using
- Your contract number, if applicable

If you are located outside the USA, contact your local distributor; see our web site (www.datatranslation.com) for the name and telephone number of your nearest distributor.

If Your Module Needs Factory Service

If your module must be returned to Data Translation, do the following:

1. Record the module's serial number, and then contact the Customer Service Department at (508) 481-3700, ext. 1323 (if you are in the USA) and obtain a Return Material Authorization (RMA).

   If you are located outside the USA, call your local distributor for authorization and shipping instructions; see our web site (www.datatranslation.com) for the name and telephone number of your nearest distributor. All return shipments to Data Translation must be marked with the correct RMA number to ensure proper processing.

2. Using the original packing materials, if available, package the module as follows:

   – Wrap the module in an electrically conductive plastic material. Handle with ground protection. A static discharge can destroy components on the module.

   – Place in a secure shipping container.

3. Return the module to the following address, making sure the RMA number is visible on the outside of the box.

   Customer Service Dept.
   Data Translation, Inc.
   100 Locke Drive
   Marlboro, MA 01752-1192

Calibration

Using the Calibration Utility

DT9862 Series modules are calibrated at the factory and should not require calibration for initial use. We recommend that you check and, if necessary, readjust the calibration of the analog input and analog output circuitry on the DT9862 Series module every six months using the DT9862 Calibration Utility.

Note: Ensure that you installed the DT9862 Series Device Driver prior to using the DT9862 Calibration Utility.

Start the DT9862 Calibration Utility as follows:

1. Click **Start** from the Task Bar.
2. Select **Programs | Data Translation, Inc | Calibration | DT9862 Calibration Utility.**
   The main menu of the DT9862 Calibration Utility appears.

Once the DT9862 Calibration Utility is running, you can calibrate the analog input circuitry (either automatically or manually), described on page 121, or the analog output circuitry of a DT9862 Series module, described on page 123.

Calibrating the Analog Input Subsystem

This section describes how to use the DT9862 Calibration Utility to calibrate the analog input subsystem of a DT9862 Series module.

The DT9862 Series module has separate calibration for each A/D input channel. You can choose to calibrate either an individual channel or all channels on the module.

Connecting a Precision Voltage Source

To calibrate the analog input circuitry for the DT9862, you need to connect an external +2.400 V precision voltage source to analog input channels 0 and 1 of the DT9862 module.

To calibrate the analog input circuitry for the DT9862S, you need to connect an external +1.150 V precision voltage source to analog input channels 0 and 1 of the DT9862S module.

Using the Auto-Calibration Procedure

Auto-calibration is the easiest to use and is the recommended calibration method. To auto-calibrate the analog input subsystem, do the following:

1. Select the **A/D Calibration** tab of the DT9862 Calibration Utility.
2. Choose either a single channel or all channels from the **Type of Calibration** drop-down list box in the **Automatic Calibration** area. If you choose all channels, analog input channel 0 is calibrated first.
3. Set the voltage supply to 0.000V.
4. Click the Auto Calibration **Start** button.
   A message appears notifying you to verify that 0.000 V is applied to the selected channel.
5. Verify that the supplied voltage to the analog input channel is 0.000 V, and then click **OK**.
   The offset value is calibrated. When the offset calibration is complete, a message appears notifying you to set the input voltage of the channel to +2.400V (for the DT9862) or +1.150 V (for the DT9862S).
6. Check that the supplied voltage to the analog input channel is +2.400 V (for the DT9862) or +1.150 V (for the DT9862S), and then click **OK**.
   The gain value is calibrated and a completion message appears.
7. If you chose to calibrate all channels, repeat steps 3 to 6 to calibrate analog input channel 1 on the module.

Note: At any time, you can click **Restore Factory Settings** to reset the A/D calibration values to their original factory settings. This process will undo any auto or manual calibration settings.

Using the Manual Calibration Procedure

If you want to manually calibrate the analog input circuitry instead of auto-calibrating it, do the following:

1. Adjust the offset for analog input channel 0 as follows:
   a. Verify that 0.000 V is applied to analog input channel 0, and that **Channel 0** is selected in the top area of the window.
   The current voltage reading for this channel is displayed in the A/D Value window.
   b. Adjust the offset by entering values between 0 and 255 in the AD0 Offset edit box, or by clicking the up/down buttons until the A/D0 Value is 0.000 V.
2. Adjust the gain for analog input channel 0 as follows:
   a. Verify that +2.400 V (for the DT9862) or +1.150 V (for the DT9862S) is applied to analog input channel 0, and that **Channel 0** is selected in the top area of the window.
   The current voltage reading for this channel is displayed in the A/D Value window.
   b. Adjust the gain by entering values between 0 and 255 in the AD0 Gain edit box, or by clicking the up/down buttons until the A/D0 Value is +2.400 V (for the DT9862) or +1.150 V (for the DT9862S).
3. Adjust the offset for analog input channel 1 as follows:
   a. Verify that 0.000 V is applied to analog input channel 1, and that **Channel1** is selected in the top area of the window.
   The current voltage reading for this channel is displayed in the A/D Value window.
   b. Adjust the offset by entering values between 0 and 255 in the AD 1 Offset edit box, or by clicking the up/down buttons until the A/D1 Value is 0.000 V.
4. Adjust the gain for analog input channel 1 as follows:
   a. Verify that +2.400 V (for the DT9862) or +1.150 V (for the DT9862S) is applied to analog input channel 1, and that **Channel 1** is selected in the top area of the window.
   The current voltage reading for this channel is displayed in the A/D Value window.
   b. Adjust the gain by entering values between 0 and 255 in the AD1 Gain edit box, or by clicking the up/down buttons until the A/D1 Value is +2.400 V (for the DT9862) or +1.150 V (for the DT9862S).

Note: At any time, you can click **Restore Factory Settings** to reset the A/D calibration values to their original factory settings. This process will undo any auto or manual calibration settings.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem."

Calibrating the Analog Output Subsystem

This section describes how to use the DT9862 Calibration Utility to calibrate the analog output subsystem of a DT9862 Series module.

To calibrate the analog output circuitry, you need to connect an external precision voltmeter to analog output channels 0 and 1 of the DT9862 Series module.

Do the following to calibrate the analog output circuitry on the DT9862 Series module:

1. Select the **D/A Calibration** tab of the DT9862 Calibration Utility.
2. Connect an external precision voltmeter to analog output channel 0 on the DT9862 Series module.
3. In the DAC Output Voltage box, select **–2.400 V**.
4. Adjust the offset by entering values between 0 and 255 in the DAC 0 Offset edit box or by clicking the up/down buttons until the voltmeter reads –2.400 V.
5. In the DAC Output Voltage box, select **2.400 V**.
6. Adjust the gain by entering values between 0 and 255 in the DAC 0 Gain edit box or by clicking the up/down buttons until the voltmeter reads 2.400 V.
7. Connect an external precision voltmeter to analog output channel 1 on the DT9862 Series module.
8. In the DAC Output Voltage box, select **–2.400 V**.
9. Adjust the offset by entering values between 0 and 255 in the DAC 1 Offset edit box or by clicking the up/down buttons until the voltmeter reads –2.400 V.
10. In the DAC Output Voltage box, select **2.400 V**.
11. Adjust the gain by entering values between 0 and 255 in the DAC 1 Gain edit box or by clicking the up/down buttons until the voltmeter reads +2.400 V.

Note: At any time, you can click **Restore Factory Settings** to reset the D/A calibration values to their original factory settings. This process will undo any D/A calibration settings.

Once you have finished this procedure, the analog output circuitry is calibrated. To close the DT9862 Calibration Utility, click the close box in the upper right corner of the window.

Specifications

Analog Input Specifications

Table 25 lists the specifications for the analog input subsystem on the DT9862 Series module.

Table 25: Analog Input Specifications

Feature	Specifications
Number of analog input channels	2 single-ended, simultaneous
Resolution	16 bits
Range DT9862: DT9862S:	 ±2.5 V ±1.25 V
Gain	1
Throughput per channel, maximum One channel (analog input only[a]): Two channels (analog input only[a]): Two channels (digital input, counter/timers, or quadrature decoders[a]): All channels (analog input, digital input, counter/timers, quadrature decoder[a]):	 10.0 MSamples/s 5.0 MSamples/s 2.0 MSamples/s 2.0 MSamples/s to onboard FIFO but limited to 415 kSamples/s continuous by USB
A/D conversion time	100 ns
Channel acquisition time ±0.5 LSB	70 ns typical
Sample-and-hold Aperture uncertainty: Aperture delay: Aperture match: Gain match: Zero match:	 200 ps typical 25 ns typical 3 ns / 500 ps typical ± 0.015% ±3 mV ± 1.5 mV
System accuracy, to % of FSR DT9862: DT9862S:	 ±0.01% ±0.1%
Bandwidth DT9862: DT9862S:	 10 MHz 300 MHz typical; 100 MHz minimum
Coupling	DC
Data encoding	Offset binary
Maximum input voltage (without damage) Power on: Power off:	 ±35 V (DT9862); ±15 V (DT9862) ±20 V (DT9862); ±10 V (DT9862)

Table 25: Analog Input Specifications (cont.)

Feature	Specifications
Input impedance DT9862: DT9862S:	 10 MΩ, 10 pF Software-controlled 50 Ω termination 500 Ω ±10%
Integral nonlinearity	< 2 LSB
Differential nonlinearity	< 1 LSB
Inherent quantizing error	1/2 LSB
Drift Zero: Gain:	 ±20 µV/°C ±20 ppm of FSR/°C
Differential linearity drift (of FSR/degree C)	±2 ppm
Input FIFO	128 kBytes[b]
Monotonicity	Yes
Effective Number of Bits (ENOBs) @ 1 kHz input	13.7 bits typical
Spurious Free Dynamic Range (SFDR) DT9862: DT9862S:	 90 dB typical 70 dB typical
ESD protection Arc: Contact:	 8 kV 4 kV

a. An analog input sample is 2 bytes, a digital input sample is 2 bytes, a counter/timer sample is 4 bytes, and a quadrature decoder sample is 4 bytes.

b. If you specify a number of samples to acquire that is less than or equal to the size of the 128 kByte input FIFO in continuous mode, you can acquire data at the maximum rate. This is called a burst. For example, you can acquire data from both analog input channels at 10 MHz in burst mode. If you specify a number of samples to acquire that is greater than the size of the input FIFO, the DT9862 Series can achieve 10 MHz when sampling one analog input channel, 5 MHz when sampling two analog input channels, or 2 MHz or less when sampling other combination of input channels. Refer to Appendix E starting on page 155 for more information on the maximum throughput for various configurations of the channel list.

Analog Output Specifications

Table 26 lists the specifications for the analog output subsystem on the DT9862 Series module.

Table 26: Analog Output Specifications

Feature	Specifications
Number of analog output channels	2 Simultaneous
Resolution	16 bits
Settling time to 0.01% of FSR	2.0 µs, 2.5 V steps 2.0 µs, 100 mV steps
Throughput, maximum	2 MSamples/s per channel (small steps < 100 mV) 500 kSamples/s per channel (full-scale steps)
Slew rate	1.25 V/µs
Glitch energy	12 nV-s, typical (essentially glitchless)
Output range	±2.5 V
Data encoding	Offset binary
Output current	±5 mA maximum load
Output impedance	0.1 Ω maximum
Capacitive driver capability	0.004 µF
Protection	Short circuit to analog ground
Integral nonlinearity	1.0 LSB / 0.5 LSB
Differential nonlinearity	1.0 LSB / 0.5 LSB
Inherent quantizing error	1.0 LSB / 0.5 LSB
Error Zero: Gain:	 Adjustable to 0 Adjustable to 0
Drift Zero (bipolar): Gain:	 ±10 ppm of FSR/°C ±30 ppm of FSR/°C
Output FIFO	256 kBytes (or 128 kSamples, total)
Monotonicity	1 LSB / Yes
ESD protection Arc: Contact:	 8 kV 4 kV

Digital I/O Specifications

Table 27 lists the specifications for the digital I/O subsystems on the DT9862 Series module.

Table 27: Digital I/O Specifications

Feature	Specifications
Number of digital I/O lines	32 (16 in, 16 out)
Number of ports	2 (16 bits each)
Logic family	LVTTL (5 V tolerant)
Logic sense	Positive true
Inputs Input type: Input logic load: High input voltage: Low input voltage: Low input current: Termination:	 Level-sensitive 1 LVTTL 2.0 V minimum 0.8 V maximum 0.4 mA maximum None
Outputs Fan out: High output: Low output: High output current: Low output current:	 12 mA 2.0 V minimum 0.8 V maximum –12 mA maximum 12 mA maximum
Interrupt on change	Yes (on first 8 bits)
Clocked with sample clock	Yes
Software I/O selectable	No

Counter/Timer and Quadrature Decoder Specifications

Table 28 lists the specifications for the counter/timer and quadrature decoder subsystems on the DT9862 Series module.

Table 28: Counter/Timer and Quadrature Decoder Subsystem Specifications

Feature	Specifications
Number of channels C/T: Quadrature decoder:	 2 3
Resolution	32 bits per channel
Minimum pulse width (minimum amount of time it takes a C/T to recognize an input pulse)	40 ns
Logic family	LVTTL (5 V tolerant)
Inputs Input logic load: High input voltage: Low input voltage: Low input current:	 1 LVTTL 2.0 V minimum 0.8 V maximum –0.4 mA maximum
Outputs Fan out: High output: Low output: High output current: Low output current:	 12 mA 2.0 V minimum 0.8 V maximum –12 mA maximum 12 mA maximum
Internal reference clock rate	50 MHz
External clock rate	25 MHz maximum

External Trigger Specifications

Table 29 lists the specifications for the external analog input and analog output triggers on the DT9862 Series module.

Table 29: External Analog Input and Analog Output Trigger Specifications

Feature	Specifications
Trigger sources Internal: External:	 Software-initiated Software-selectable
Input type	Edge-sensitive
Logic family	LVTTL (5 V tolerant)
Inputs Input logic load: Input termination: High input voltage: Low input voltage: Low input current:	 1 LVTTL 2.2 kΩ pull-up to +3.3 V 2.0 V minimum 0.8 V maximum –0.25 mA maximum
Minimum pulse width High: Low:	 25 ns 25 ns
Triggering modes Single scan: Continuous scan:	 Yes Yes

Internal Clock Specifications

Table 30 lists the specifications for the internal analog input and analog output clocks on the DT9862 Series module.

Table 30: Internal Analog Input and Analog Output Clock Specifications

Subsystem	Feature	Specifications
Analog input	Reference frequency	100 MHz
	Frequency range	1.526 kHz to 16.67 MHz
	Usable frequency range	500 kHz to 10 MHz
	Period range	655.3 µs to 60 ns
	Usable period range	2 µs to 100 ns
Analog output	Reference frequency	50 MHz
	Frequency range	0.01164 Hz to 16.67 MHz
	Usable frequency range	0.01164 Hz to 2 MHz
	Period range	85.89 s to 60 ns
	Usable period range	85.89 s to 500 ns

External Clock Specifications

Table 31 lists the specifications for the external analog input and analog output clocks on the DT9862 Series module.

Table 31: External Analog Input and Analog Output Clock Specifications

Feature	Specifications
Input type	Edge-sensitive, rising- or falling-edge progammable. The clock must be free running and remain at a constant frequency.
Logic family	LVTTL (5 V tolerant)
Inputs Input logic load: Input termination: High input voltage: Low input voltage:	 1 LVTTL 2.2 kΩ pull-up to +3.3 V 2.0 V 0.8 V
A/D Frequency	500 kHz to 10.0 MHz (reduced accuracy below 1 MHz)
Duty cycle (A/D)	45/55%
D/A Frequency	DC to 2 MHz
Minimum pulse width (D/A) High: Low:	 25 ns 25 ns

Power, Physical, and Environmental Specifications

Table 32 lists the power, physical, and environmental specifications for the DT9862 Series module.

Table 32: Power, Physical, and Environmental Specifications

Feature	Specifications
Power, +5 V	±5% @ 2 A maximum
Physical Dimensions -Enclosure Width: Length: Height: Weight (DT9862-2-2):	 8.380 inches (212.85 mm) 9.319 inches (236.7 mm) 1.720 inches (43.69 mm) 35.44 ounces (1004.5 g)
Physical Dimensions - OEM Version Width: Length: Height: Weight (DT9862-2-2 OEM version):	 7.848 inches (199.34 mm) 9.18 inches (233.17 mm) 0.85 inches (21.59 mm) 14.12 ounces (400.5 g)
Environmental Operating temperature range: Storage temperature range: Relative humidity: Altitude:	 0° C to 55° C –25° C to 85° C to 95%, noncondensing to 10,000 feet

Connector Specifications

Table 33 lists the specifications for the connectors on the DT9862 Series module and the STP78 screw terminal panel.

Table 33: Connector Specifications

Module/Panel	Connector	Part Number on Module (or Equivalent)	Mating Cable Connector
DT9862 Series Module	SMA connectors (J1 to J4; J7 to J10)	Amphenol Connex 132203	Amphenol Connex 132125
	5 V In (J5)	Kycon KPJX-4S-S	Kycon KPPX-4P
	USB (J6)	Amp/Tyco 292304-2	Standard USB cable
	I/O (J11)	FCI 10090927-S786XLF	FCI 10090769-P786ALF
	Secondary power connector (TB1)	Amphenol/PCD ELVH03500	Amphenol/PCD ELVP03100
STP78 Screw Terminal Panel	I/O (J1)	FCI 10090927-S786XLF	FCI 10090769-P786ALF

Regulatory Specifications

Table 34 lists the regulatory specifications for the DT9862 Series modules.

Table 34: Regulatory Specifications

Feature	Specifications
Emissions (EMI)	FCC Part 15, Class A EN55011:2007 (Based on CISPR-11, 2003/A2, 2006)
Immunity	EN61326-1:2006 Electrical Equipment for Measurement, Control, and Laboratory Use EMC Requirements EN61000-4-2:2001 Electrostatic Discharge (ESD) 4 kV contact discharge, 8 kV air discharge, 4 kV horizontal and vertical coupling planes EN61000-4-3:2002 Radiated electromagnetic fields, 3 V/m, 80 to 1000 MHz; 3 V/m, 1.4 GHz to 2 GHz; 1 V/m, 2 GHz to 2.7 GHz EN61000-4-4:2004 Electrical Fast Transient/Burst (EFT) 1 kV on data cables EN61000-4-6:2003 Conducted immunity requirements, 3 Vrms on data cables 150 kHz to 80 MHz
RoHS (EU Directive 2002/95/EG)	Compliant (as of July 1st, 2006)

External Power Supply Specifications

Table 35 lists the specifications for the EP361 +5 V external power supply that is used with the DT9862 Series modules.

Table 35: External Power Supply (EP361) Specifications

Feature	Specifications
Type	Total Power medical power supply (TPES22-050400 or TPEMG24-S050400-7)
Input voltage	Typical 90 - 264 V AC
Input current TPES22-050400 TPEMG24-S050400-7	 Typical 0.38 A at 115 V AC, 0.15 A at 230 V AC Typical 0.347 A at 115 V AC, 0.215 A at 230 V AC
Frequency	47 to 63 Hz
Inrush current TPES22-050400 TPEMG24-S050400-7	 35 A at 230 V AC typical or less than 30 A by adding thermistor 6.274 A RMS at 230 V AC
Output voltage	5 V DC
Output current	4.0 A
Output wattage TPES22-050400 TPEMG24-S050400-7	 Typical 22 - 24 W Typical 20 - 24 W
Noise and ripple	1% peak to peak
Regulatory specifications TPES22-050400 TPEMG24-S050400-7	 UL, N, CE, FCC Class B UL, ITE, CE, FCC Class B, Energy Star compliant

Pin Assignments

Connectors on the DT9862 Series Modules

This section describes the pin assignments for the connectors on the DT9862 Series module.

I/O Connector (J11)

Figure 29 shows the layout of the I/O connector (J11) on the DT9862 Series module.

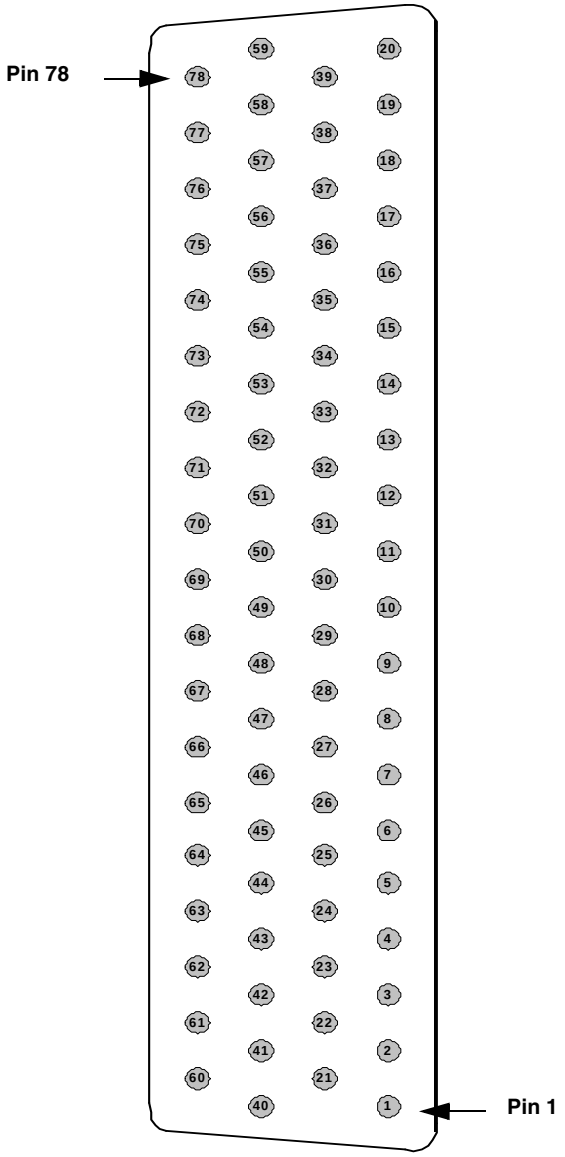


Figure 29: Layout of the 78-Pin I/O Connector

Table 36 lists the pin assignments for the I/O connector on the DT9862 Series module.

Table 36: Pin Assignments for the I/O Connector (J11) on the DT9862 Series Module

Connector Pin Number	Signal Description	Connector Pin Number	Signal Description
1	Quad Dec 1 Index	40	Digital Ground
2	Digital Ground	41	Digital Output 0
3	Quad Dec 1 B	42	Digital Output 1
4	Digital Ground	43	Digital Output 2
5	Quad Dec 1 A	44	Digital Output 3
6	Digital Ground	45	Digital Output 4
7	Quad Dec 0 Index	46	Digital Output 5
8	Digital Ground	47	Digital Output 6
9	Quad Dec 0 B	48	Digital Output 7
10	Digital Ground	49	Digital Output 8
11	Quad Dec 0 A	50	Digital Output 9
12	Digital Ground	51	Digital Output 10
13	Counter 0 Out	52	Digital Output 11
14	Digital Ground	53	Digital Output 12
15	Counter 0 Gate	54	Digital Output 13
16	Digital Ground	55	Digital Output 14
17	Counter 0 Clock	56	Digital Output 15
18	Digital Ground	57	Digital Ground
19	+5 V Output	58	Digital Ground
20	+5 V Output Ground	59	Digital Ground
21	Quad Dec 2 Index	60	Digital Ground
22	Digital Ground	61	Digital Input 0
23	Quad Dec 2 B	62	Digital Input 1
24	Digital Ground	63	Digital Input 2
25	Quad Dec 2 A	64	Digital Input 3
26	Digital Ground	65	Digital Input 4
27	Counter 1 Output	66	Digital Input 5
28	Digital Ground	67	Digital Input 6
29	Counter 1 Gate	68	Digital Input 7
30	Digital Ground	69	Digital Input 8

Table 36: Pin Assignments for the I/O Connector (J11) on the DT9862 Series Module (cont.)

Connector Pin Number	Signal Description	Connector Pin Number	Signal Description
31	Counter 1 Clock	70	Digital Input 9
32	Digital Ground	71	Digital Input 10
33	Reserved	72	Digital Input 11
34	Reserved	73	Digital Input 12
35	Reserved	74	Digital Input 13
36	Reserved	75	Digital Input 14
37	Reserved	76	Digital Input 15
38	Reserved	77	Digital Ground
39	Digital Ground	78	Digital Ground

External USB Connector (J6)

Figure 30 shows the layout of the external USB connector (J6) on the DT9862 Series module.

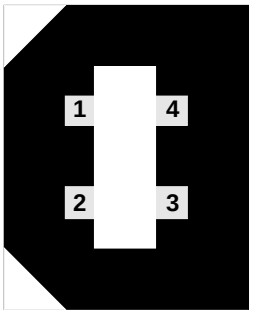


Figure 30: Layout of the USB Connector

Table 37 lists the pin assignments for the USB connector on the DT9862 Series module.

Table 37: Pin Assignments for the USB Connector (J6) on the DT9862 Series Module

Connector Pin Number	Signal Description	Connector Pin Number	Signal Description
1	USB +5 V	3	USB Data +
2	USB Data –	4	USB Ground

Internal USB Header

Figure 31 shows the layout of the internal USB header on the OEM version of the DT9862 Series module.

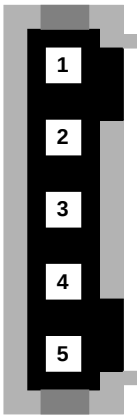


Figure 31: Layout of the Internal USB Header on the OEM Version of the DT9862 Series Module

Table 38 lists the pin assignments for the internal USB header on the OEM version of the DT9862 Series module.

Table 38: Pin Assignments for the USB Connector on the OEM Version of DT9862 Series Module

Connector Pin Number	Signal Description	Connector Pin Number	Signal Description
1	USB +5 V	4	USB Ground
2	USB Data –	5	USB Shield (Chassis)
3	USB Data +		

Note: The USB external connection must be properly shielded and terminated per USB specification requirements.

External +5 V Connector (J5)

Figure 32 shows the layout of the external +5 V connector (J5) on the DT9862 Series module.

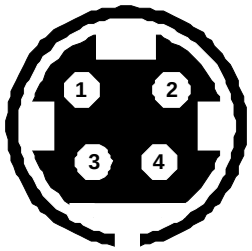


Figure 32: Layout of the External +5 V Connector

Table 39 lists the pin assignments for the external +5 V connector on the DT9862 Series module.

Table 39: Pin Assignments for the External +5 V Connector (J5) on the DT9862 Series Module

Connector Pin Number	Signal Description	Connector Pin Number	Signal Description
1	+5 V	3	Ground
2	+5 V	4	Ground

Internal +5 V Header (TB1)

The OEM version of the DT9862 Series module provides a secondary power connector (TB1), which is useful for embedded applications. The location of the connector is shown on page 39.

Figure 32 shows the layout of the internal +5 V internal header (TB1) on the OEM version of the DT9862 Series module.

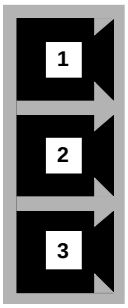


Figure 33: Layout of the +5 V Internal Header (TB1) on the OEM version of the DT9862 Series Module

Table 40 lists the pin assignments for the +5 V internal header on the OEM version of the DT9862 Series module for connecting an external power supply.

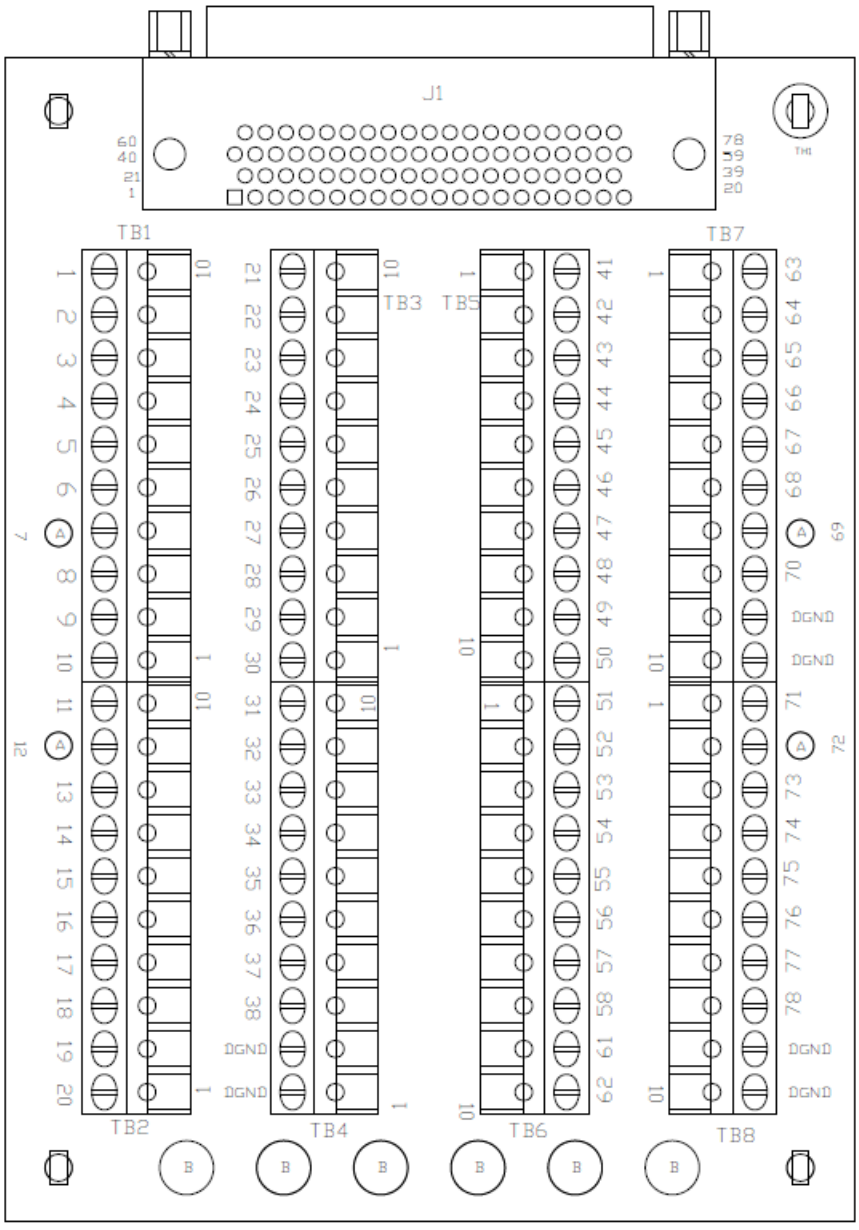
Table 40: Pin Assignments for the +5 V Header (TB1) on the OEM Version of the DT9862 Series Module

Connector Pin Number	Signal Description	Connector Pin Number	Signal Description
1	+5 V	3	Shield (Chassis)
2	Ground		

STP78 Screw Terminal Panel

To make digital connections easier, you can connect the STP78 screw terminal panel to the 78-pin, I/O connector on the DT9862 Series module using the EP390 cable.

Figure 34 shows the layout of the STP78 screw terminal panel.



Notes:
1. You can use holes marked "A" for DIN-rail mounting.
2. You can use holes marked "B"to tie down wires.

Figure 34: Layout of the STP78 Screw Terminal Panel

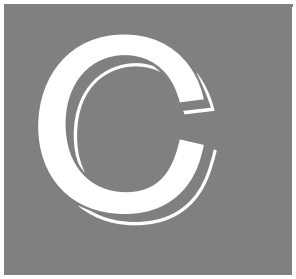
Table 41 lists the assignments for each screw terminal on the STP78 screw terminal panel.

Table 41: Screw Terminal Assignments for the STP78

Screw Terminal	Terminal Block Position	Signal Description	Screw Terminal	Terminal Block Position	Signal Description
1	TB1, 10	Quad Dec 1 Index	41	TB5, 1	Digital Output 0
2	TB1, 9	Digital Ground	42	TB5, 2	Digital Output 1
3	TB1, 8	Quad Dec 1 B	43	TB5, 3	Digital Output 2
4	TB1, 7	Digital Ground	44	TB5, 4	Digital Output 3
5	TB1, 6	Quad Dec 1 A	45	TB5, 5	Digital Output 4
6	TB1, 5	Digital Ground	46	TB5, 6	Digital Output 5
7	TB1, 4	Quad Dec 0 Index	47	TB5, 7	Digital Output 6
8	TB1, 3	Digital Ground	48	TB5, 8	Digital Output 7
9	TB1, 2	Quad Dec 0 B	49	TB5, 9	Digital Output 8
10	TB1, 1	Digital Ground	50	TB5, 10	Digital Output 9
11	TB2, 10	Quad Dec 0 A	51	TB6, 1	Digital Output 10
12	TB2, 9	Digital Ground	52	TB6, 2	Digital Output 11
13	TB2, 8	Counter 0 Out	53	TB6, 3	Digital Output 12
14	TB2, 7	Digital Ground	54	TB6, 4	Digital Output 13
15	TB2, 6	Counter 0 Gate	55	TB6, 5	Digital Output 14
16	TB2, 5	Digital Ground	56	TB6, 6	Digital Output 15
17	TB2, 4	Counter 0 Clock	57	TB6, 7	Digital Ground
18	TB2, 3	Digital Ground	58	TB6, 8	Digital Ground
19	TB2, 2	+5 V Output	59	TB6, 9	Digital Input 0
20	TB2, 1	+5 V Output Ground	60	TB6, 10	Digital Input 1
21	TB3, 10	Quad Dec 2 Index	61	TB7, 1	Digital Input 2
22	TB3, 9	Digital Ground	62	TB7, 2	Digital Input 3
23	TB3, 8	Quad Dec 2 B	63	TB7, 3	Digital Input 4
24	TB3, 7	Digital Ground	64	TB7, 4	Digital Input 5
25	TB3, 6	Quad Dec 2 A	65	TB7, 5	Digital Input 6
26	TB3, 5	Digital Ground	66	TB7, 6	Digital Input 7
27	TB3, 4	Counter 1 Output	67	TB7, 7	Digital Input 8
28	TB3, 3	Digital Ground	68	TB7, 8	Digital Input 9
29	TB3, 2	Counter 1 Gate	69	TB7, 9	Digital Ground
30	TB3, 1	Digital Ground	70	TB7, 10	Digital Ground

Table 41: Screw Terminal Assignments for the STP78 (cont.)

Screw Terminal	Terminal Block Position	Signal Description	Screw Terminal	Terminal Block Position	Signal Description
31	TB4, 10	Counter 1 Clock	71	TB8, 1	Digital Input 10
32	TB4, 9	Digital Ground	72	TB8, 2	Digital Input 11
33	TB4, 8	Reserved	73	TB8, 3	Digital Input 12
34	TB4, 7	Reserved	74	TB8, 4	Digital Input 13
35	TB4, 6	Reserved	75	TB8, 5	Digital Input 14
36	TB4, 5	Reserved	76	TB8, 6	Digital Input 15
37	TB4, 4	Reserved	77	TB8, 7	Digital Ground
38	TB4, 3	Reserved	78	TB8, 8	Digital Ground
39	TB4, 2	Digital Ground	79	TB8, 9	Digital Ground
40	TB4, 1	Digital Ground	80	TB8, 10	Digital Ground



Ground, Power, and Isolation

Figure 35 illustrates how ground, power, and isolation are connected on a DT9862 Series module.

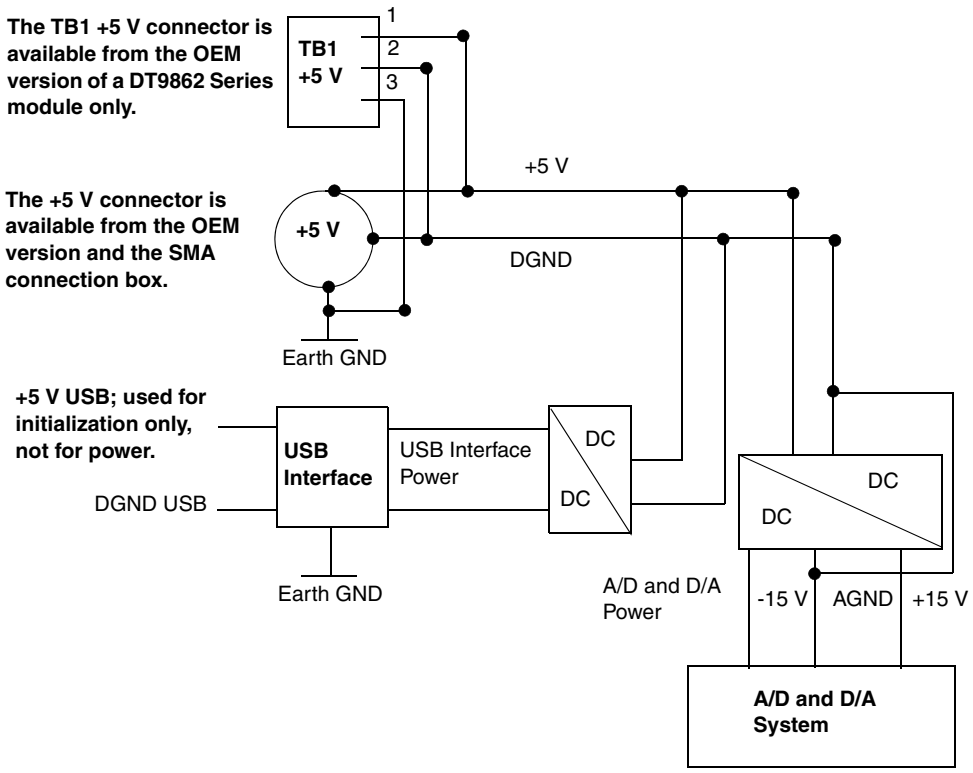


Figure 35: Ground, Power, and Isolation Connections

Keep the following in mind:

- Earth ground on the DT9862 Series module is not connected to DGND or AGND.
- Earth ground is connected to the aluminum case of the SMA connection box.
- You should connect earth ground to the power supply earth.
- You should isolate the +5V/DGND input. Note that the EP361 power supply (shipped with the SMA connection box and available from Data Translation for the OEM version of the module) has no connection between +5V/DGND and earth ground.
- The USB connector case is connected to earth ground.
- The USB data lines and USB GND are not connected to earth ground.
- The USB DGND is connected to the USB GND of the PC USB port.

Register-Level Programming

Reading the Setting for the Current Termination Resistor

To read the setting for the 50 Ω current termination resistor on the DT9862 module programmatically (rather than in the Open Layers Control Panel), you can use the Data Acq SDK function **olDiagReadReg**, as follows:

```
#define RESISTOR_TERMINATION_VREG 0x4005
ULONG ResistorTerminationMask;
//bit<0> is for channel 0, bit <1> is for channel 1
//A bit value of 1 means the register is enabled.
//A bit value of 0 means the register is disabled.
olStatus = olDiagReadReg(m_hDev, RESISTOR_TERMINATION_VREG,
   &ResistorTerminationMask, 1);
```

Refer to page 33 for more information on the Open Layers Control Panel.

Changing the Setting for the Current Termination Resistor

To change the setting for the 50 Ω current termination resistor on the DT9862 module programmatically (rather than using the Open Layers Control Panel), use the Data Acq SDK function **olDiagWriteReg**, as follows:

```
#define RESISTOR_TERMINATION_VREG 0x4005
ULONG ResistorTerminationMask;
//bit<0> is for channel 0, bit <1> is for channel 1
//A bit value of 1 means the register is enabled.
//A bit value of 0 means the register is disabled.
olStatus = olDiagWriteReg(m_hDev, RESISTOR_TERMINATION_VREG,
   ResistorTerminationMask, 1);
```

Writing to this register updates the setting for the current termination resistor on the next configuration or driver load, such as a system reboot. Changes to this setting remain even if the device is power cycled.

Refer to page 33 for more information on the Open Layers Control Panel.

Sample Frequencies and Data Rates to the Host

Table 42 shows the maximum sampling frequencies and data rates to the host that can be achieved with various configurations of the input channel list.

Table 42: Maximum Sampling Frequencies and Data Rates to the Host for Various Channel List Configurations

Input Channel List Configuration	Maximum Sampling Frequency	Maximum Data Rate to Host
1 analog input channel (either channel 0 or channel 1)	10 MHz	20 MB/s
2 analog input channels	5 MHz[a]	28.57 MB/s
2 analog input channels (burst mode)	10 MHz[b]	28.57 MB/s
digital input channel only	2.5 MHz	5 MB/s
1 analog input channel + digital input	2.5 MHz	10 MB/s
2 analog input channels + digital input	2.5 MHz	15 MB/s
1 counter/timer	2.5 MHz	10 MB/s
1 analog input channel + 1 counter/timer	2.5 MHz	15 MB/s
2 analog input channels + 1 counter/timer	2.5 MHz	20 MB/s
digital input + 1 counter/timer	2.5 MHz	15 MB/s
1 analog input channel + digital input + 1 counter/timer	2.5 MHz	20 MB/s
2 analog input channels + digital input + 1 counter/timer	2.0 MHz[a]	25 MB/s
2 counter/timers	2.5 MHz	20 MB/s
1 analog input channel + 2 counter/timers	2.0 MHz[a]	25 MB/s
2 analog input channels + 2 counter/timers	1.67 MHz[a]	24 MB/s
digital input + 2 counter/timers	2.0 MHz[a]	25 MB/s
1 analog input channel + digital input + 2 counter/timers	1.67 MHz[a]	25 MB/s
2 analog input channels + digital input + 2 counter/timers	1.43 MHz[a]	25 MB/s
1 quad decoder	2.5 MHz	10 MB/s
1 analog input channel + 1 quad decoder	2.5 MHz	15 MB/s
1 analog input channel + digital input + 1 quad decoder	2.5 MHz	20 MB/s
1 analog in channel + digital in + 1 counter/timer + 1 quad decoder	1.67 MHz[a]	25 MB/s
1 analog in channel + digital in + 2 counter/timers + 1 quad decoder	1.25 MHz[a]	25 MB/s
2 analog input channel + 1 quad decoder	2.5 MHz	20 MB/s
2 analog input channel + digital input + 1 quad decoder	2.0 MHz[a]	25 MB/s
2 analog in channel + digital in + 1 counter/timer + 1 quad decoder	1.43 MHz[a]	25 MB/s
2 analog in channel + digital in + 2 counter/timers + 1 quad decoder	1.43 MHz[a]	25 MB/s
2 quad decoders	2.5 MHz	20 MB/s
1 analog input channel + 2 quad decoders	2.0 MHz[a]	25 MB/s

Table 42: Maximum Sampling Frequencies and Data Rates to the Host for Various Channel List Configurations

Input Channel List Configuration	Maximum Sampling Frequency	Maximum Data Rate to Host
1 analog input channel + digital in + 2 quad decoders	1.67 MHz[a]	25 MB/s
1 analog in channel + digital in + 1 counter/timer + 2 quad decoders	1.25 MHz[a]	25 MB/s
1 analog in channel + digital in + 2 counter/timers + 2 quad decoders	1.0 MHz[a]	25 MB/s
2 analog input channel + 2 quad decoders	1.67 MHz[a]	25 MB/s
2 analog input channel + digital in + 2 quad decoders	1.43 MHz[a]	25 MB/s
2 analog in channel + digital in + 1 counter/timer + 2 quad decoders	1.43 MHz[a]	25 MB/s
2 analog in channel + digital in + 2 counter/timers + 2 quad decoders	0.91 MHz[a,c]	25 MB/s
3 quad decoder	1.67 MHz[a]	25 MB/s
1 analog input channel + 3 quad decoders	1.43 MHz[a]	25 MB/s
1 analog input channel + digital in + 3 quad decoders	1.25 MHz[a]	25 MB/s
1 analog in channel + digital in + 1 counter/timer + 3 quad decoders	1.0 MHz[a]	25 MB/s
1 analog in channel + digital in + 2 counter/timers + 3 quad decoders	0.83 MHz[a,c]	25 MB/s
2 analog in channel + 3 quad decoders	1.25 MHz[a]	25 MB/s
2 analog in channel + digital in + 3 quad decoders	1.43 MHz[a]	25 MB/s
2 analog in channel + digital in + 1 counter/timer + 3 quad decoders	0.91MHz[a,c]	25 MB/s
2 analog in channel + digital in + 2 counter/timers + 3 quad decoders	0.91 MHz[a,c]	25 MB/s

a. Higher rates have been attained with an optimized system. The streaming data rate is system and application dependent.
b. Both channels captured in the FIFO at 10 MHz. Maximum acquire time for 2 analog input channels is 3.2768 ms. Sampling frequency formula: (sampling frequency x number of channels)/1 x 65536. This is a subset of continuous acquire (the number of samples is less than or equal to the size of the input FIFO). The size of the input FIFO is 128 kBytes, where analog input and digital input sample s are 2 bytes, and counter/timer and quadrature decoder samples are 4 bytes.
c. Sampling frequencies below 1 MHz can reduce accuracy.

Digitizing and Sampling

Introduction

This appendix reprints a white paper that was written by Hideo Okawara of Verigy Japan, in December of 2008, entitled "Mixed Signal Lecture Series DSP-Based Testing -- Fundamentals 8 Under Sampling".

It is presented here to give more background information about the difference between digitizing and sampling.

Preface to the Series

ADC and DAC are the most typical mixed signal devices. In mixed signal testing, the analog stimulus signal is generated by an arbitrary waveform generator (AWG) which employs a D/A converter inside, and the analog signal is measured by a digitizer or a sampler which employs an A/D converter inside. The stimulus signal is created with mathematical method, and the measured signal is processed with mathematical method, extracting various parameters. It is based on digital signal processing (DSP) so that our test methodologies are often called DSP-based testing.

Test/application engineers in the mixed signal field should have a thorough knowledge about DSP-based testing. FFT (Fast Fourier Transform) is the most powerful tool here. This corner will deliver a series of fundamental knowledge of DSP-based testing, especially FFT and its related topics. It will help test/application engineers comprehend what the DSP-based testing is and assorted techniques.

Under-Sampling

You may remember one of the fundamental theories discussed in the first article -- “Nyquist Theory.” If your signal is band-limited, when you would sample it with the frequency more than twice the maximum frequency of the band, all characteristic information of the signal is stored in the discrete time data stream. In other words, if the sampling frequency is lower than twice the bandwidth, something would be lost. This condition is called “under-sampling,” which is the theme of this article.

Digitizer and Sampler

In the V93000 SOC test system, there are two kinds of analog measurement instruments available. One is called a digitizer and the other is a sampler. Both of them employ A/D converters inside.

A digitizer takes care of signals that conform the Nyquist theory. A sampler measures signals that may exceed more than the half of the sampling frequency.

Figure 1 shows a typical block diagram of a digitizer. The input signal first goes through a LPF called “anti-aliasing filter”, and the band-limited signal is quantized or digitized by the A/D converter. The sampling frequency in the digitizer should be greater than twice the cut-off frequency of the anti-aliasing filter to conform to the Nyquist theory. The digitized data array is stored in the waveform memory. The data will be processed to derive required test parameters by various DSP operations in the tester controller. The input analog bandwidth is specified by the anti-aliasing filter and the real time sampling frequency of the ADC. In general today’s mixed signal testers employ the order of 100Msps 16-bit digitizer. Digitizing oscilloscopes employ the order of >1Gsps 8-bit digitizer.

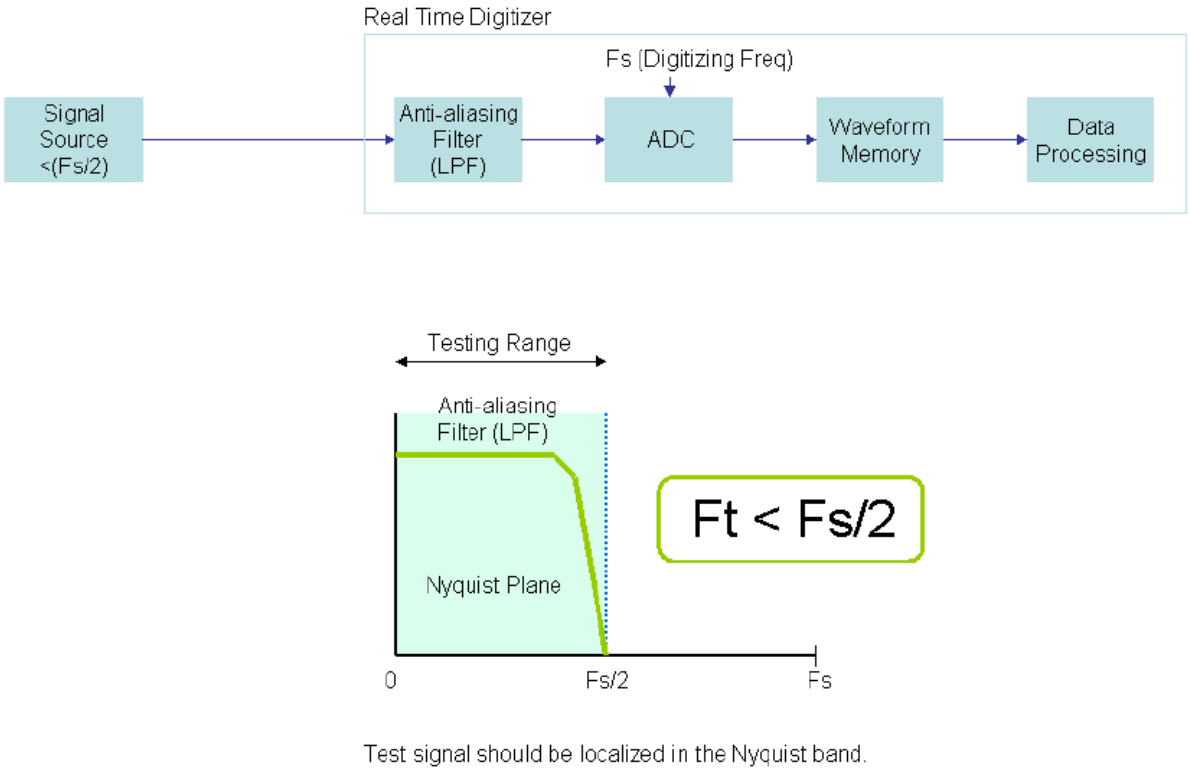


Figure 1: Digitizer

Figure 2 shows a typical block diagram of a sampler. The difference with the digitizer is that there is no anti-aliasing filter integrated but the sampling head, or track-and-hold device, is employed at the front end. The input analog bandwidth is specified by the performance of the sampling head, which is usually several GHz. The input signal path should have adequate bandwidth.

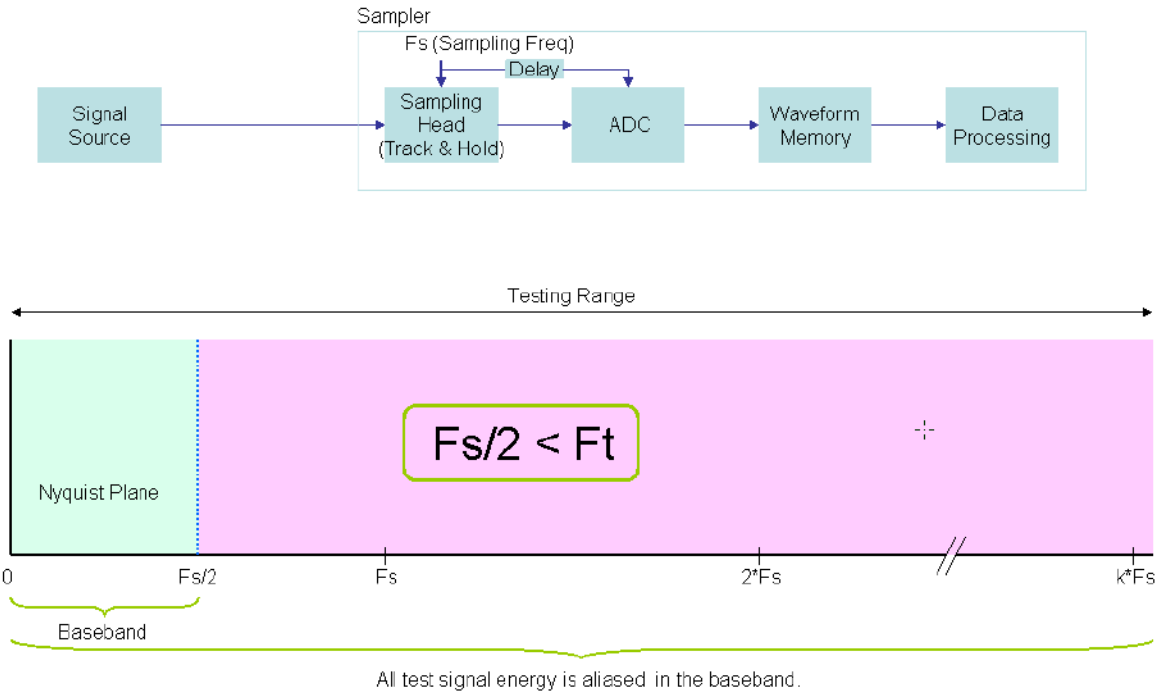


Figure 2: Sampler

Aliasing

"Aliasing" is often mentioned in the discussion about waveform digitizers and samplers. Aliasing is not a good thing in normal digitizing operations. It should be avoided for signal analyses. The Nyquist theory must be followed to the letter especially for signal to noise ratio (S/N). On the other hand, aliasing is the main player in the under-sampling condition. Figure 3 describes about the frequency domain of 8 points of sampled data (N=8). There are N/2=4 bin locations in the baseband area or the Nyquist plane. The bin locations more than N/2(=4) are folded and degenerated in the baseband page as depicted. This phenomenon is called "aliasing."

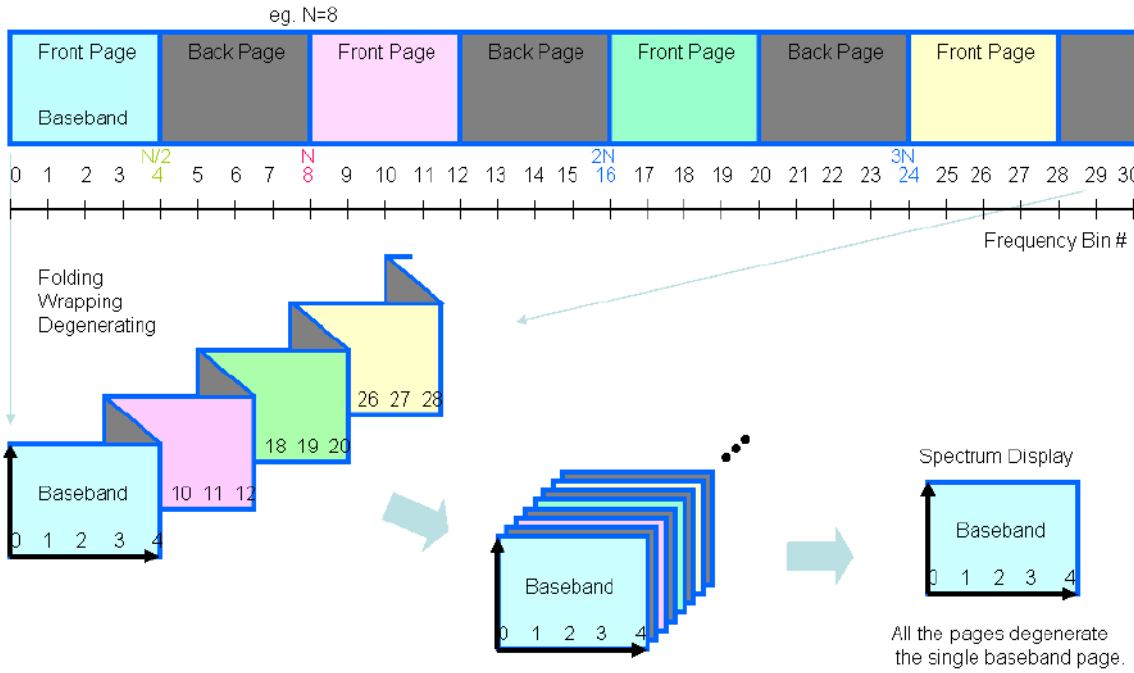


Figure 3: Aliasing

You can see the single baseband page as the frequency domain display, but this page actually contains entire information in higher pages and the display is the mixture of them. The planes labeled as "Front Page" in the picture are transparent on the baseband page in the normal direction, but the planes labeled as "Back Page" are transparent inside out. You can see the baseband page only, but you see mixture of all pages. Therefore once aliasing occurs, you cannot tell how the original spectrum looks without enough knowledge about the signal in advance.

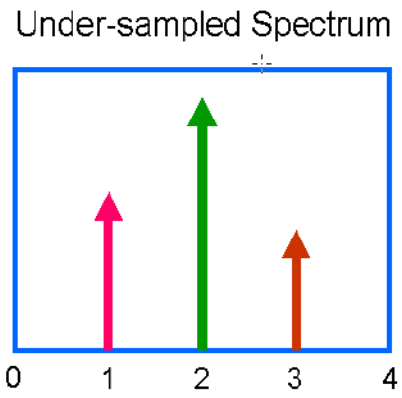


Figure 4: Spectrum

When you see the spectrum as Figure 4 in under-sampling situation, you might think that the original spectral lines are located at the bins #25, 26, 27 as Figure 5.

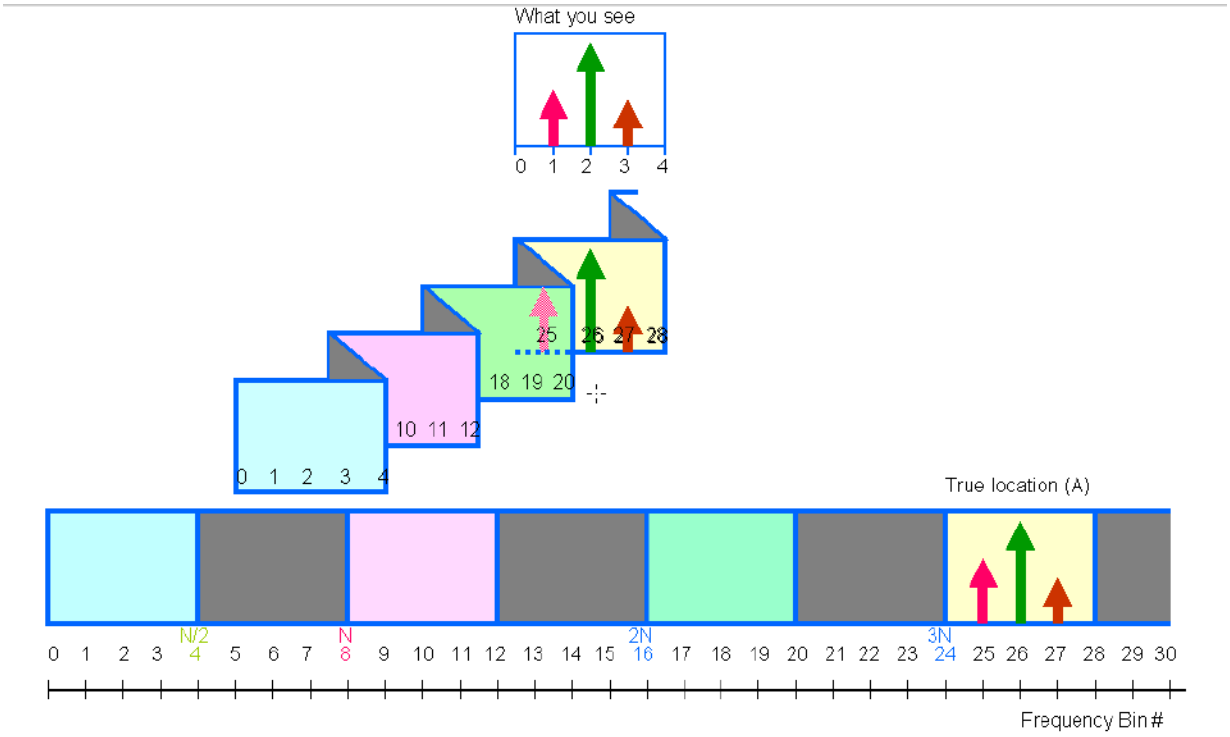


Figure 5: Original Signal Location (A)

However, the true signal location may be located at the bins #1, 19, 26 as Figure 6 shows. Both situations result in the same spectrum as Figure 4.

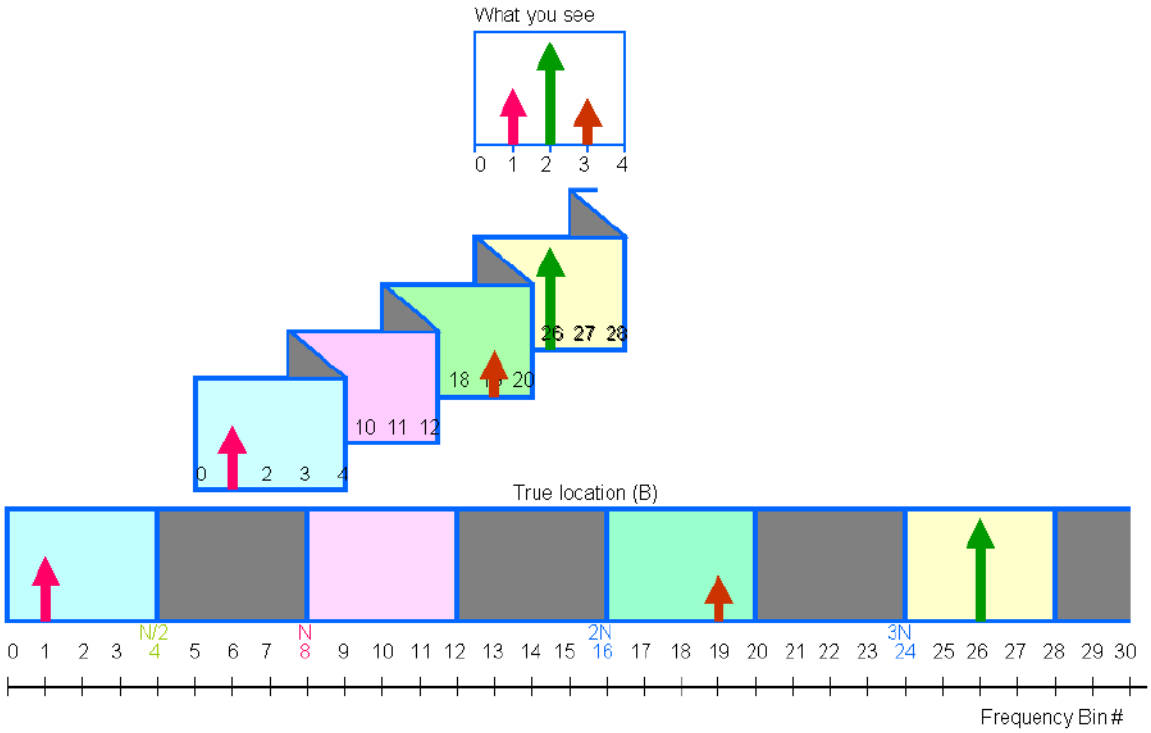


Figure 6: Original Signal Location (B)

Now that you understand what could happen when violating the Nyquist theory. When you do sampling that violates the Nyquist theory, it is called “under-sampling,” which consequently loses something. The frequency information is lost. However, in the mixed signal testing arena, the stimulus signal is created by you, and is supplied to the DUT. The signal is well known to you. Therefore you can locate which spectrum corresponds to the test signal you applied with a simple math system.

Coherent Condition

The coherent condition is the key to successful measurement in the DSP-based testing. It is described Ft/Fs=M/N, where Ft is the test signal frequency, Fs is the sampling frequency, M is the number of test signal cycles, and N is the number of data. When under-sampling, Ft>Fs/2 so that M>N/2. Consequently in the under-sampling situation, the coherent condition can be extended as follows.

$$\frac{Ft}{Fs} = \frac{M}{N} = K + \frac{Mx}{N}$$

Ft: Signal Frequency M: Number of Cycles K: Zone Number

Fs: Sampling Frequency N: Number of Points Mx: Aliased Bin Number (1)

M and N must be integer numbers, and should be mutually prime. This rule is inherited to Mx and N combination. Mx should be between –N/2 and N/2. Usually N is 2^n for convenience of FFT so that Mx is an odd number.

The coherent equation (1) is related to the degenerated spectrum as Figure 7. The point is the aliasing bin number Mx, which is between –N/2 and N/2. If Mx>0, then the signal is located in the front page. If Mx<0, then the signal is located in the back page. Consequently |Mx| indicates where the aliased signal would fall in the baseband. When you make up your test condition with under-sampling, you may want to set up your spectrum appearance as you like. Usually Ft and N are settled at first so that you would have freedom to decide Fs and Mx. If you can control Fs, you can adjust Mx for your favorite location. You should keep in mind the relationship described in Figure 7. Generally speaking, a mixed signal tester must have at least two master clock domains. Probably the test frequency Ft would be based on one master clock domain. Then the sampling frequency Fs requires taking the other master clock domain for being precisely set up. Otherwise you could not settle your test condition coherently.

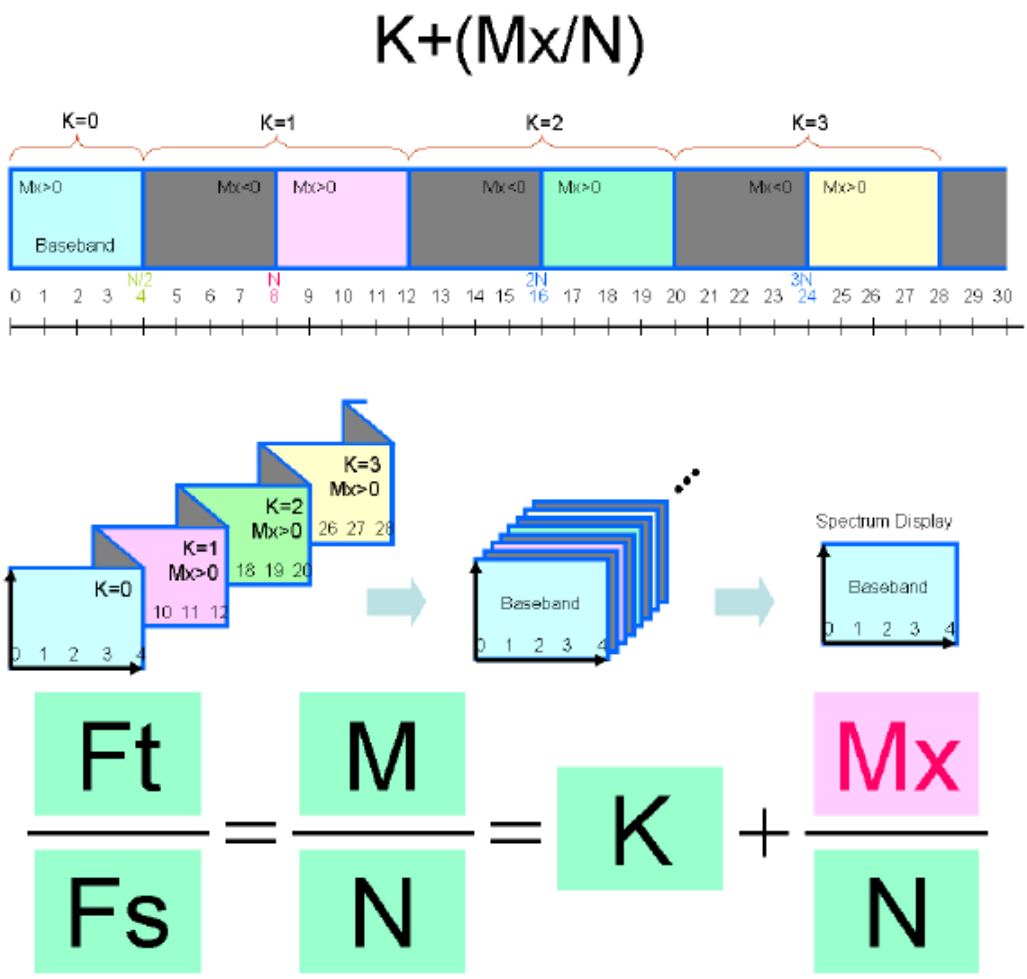


Figure 7: Coherent Equation vs Degenerated Spectrum

Waveform Reconstruction

There is a clock waveform whose frequency is Ft. Let's see a normal sampling (digitizing) situation. The signal is sampled by the 16 times higher sampling frequency Fs. (Fs=16Ft) A single clock waveform is digitized with 16 points of data (N=16) as Figure 8. The captured data automatically replicates the original clock waveform. In this case, the coherent equation is Ft/Fs=1/16 so that M/N=1/16.

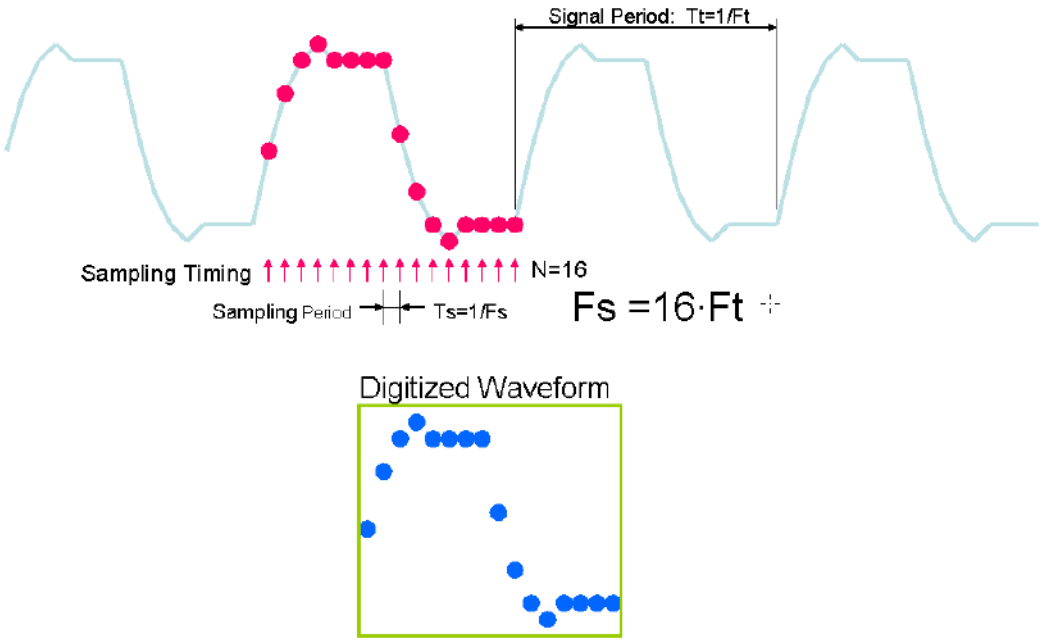


Figure 8: Normal Sampling/Digitizing (1)

The next digitizing situation is in Figure 9. The three cycles of the clock waveform is digitized with 16 points of data so that the coherent equation is Ft/Fs=3/16 and M/N=3/16. In this case the digitized data consists of 3 cycles of the primitive waveform. When you apply DSP_SHUFFLE(3 cycles), a single cycle of the original waveform can be replicated as Figure 9.

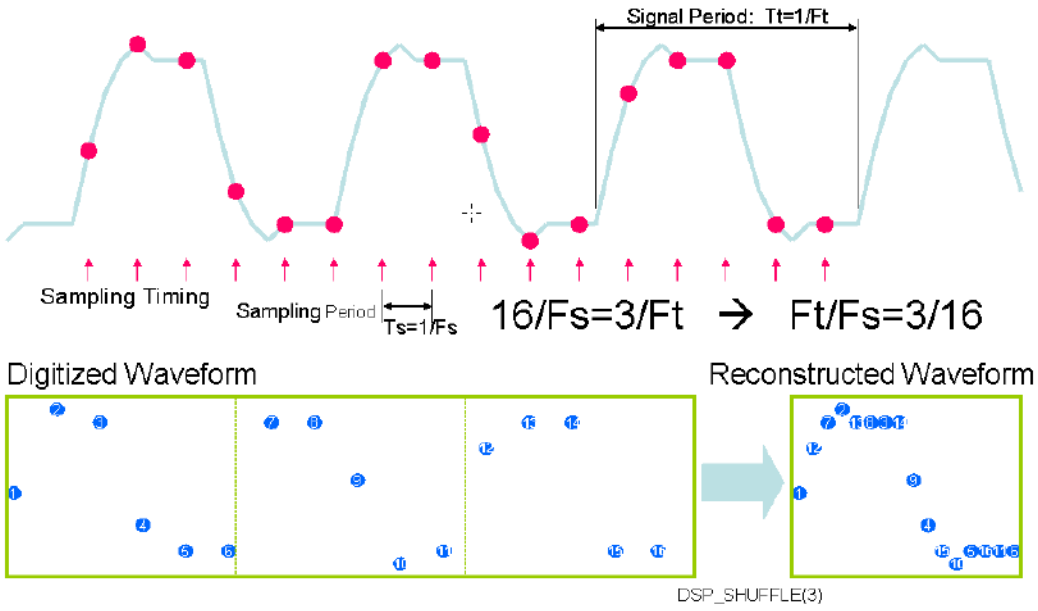


Figure 9: Normal Sampling/Digitizing (2)

Let's move on to the under-sampling situation. (Figure 10). Each sampling point sweeps over the primitive clock waveform step by step. When 16-sampling completes, the sampled data directly replicates a single cycle of the original clock waveform. The coherent equation becomes Ft/Fs=2+1/16. Then M/N=K+Mx/N=2+1/16. Mx=1 here.

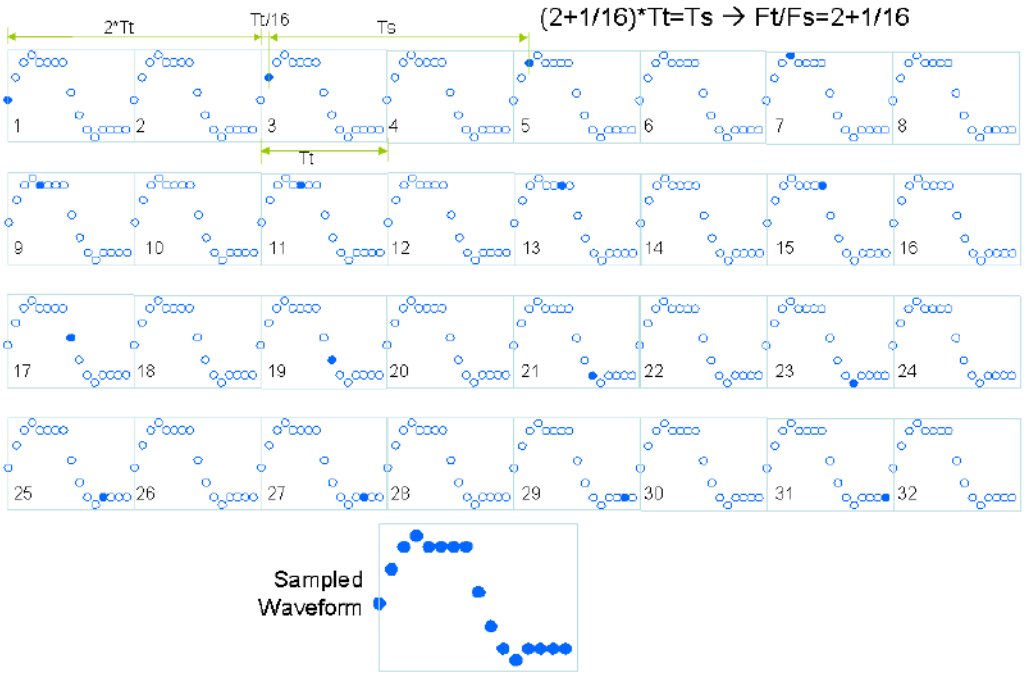


Figure 10: Under-sampling (1)

Next under-sampling in Figure 11 is Ft/Fs=2+3/16. So M/N=K+Mx/N=2+3/16. Then Mx=3. The three cycles of the primitive waveform is sampled so that DSP_SHUFFLE(3 cycles) can replicate a single cycle of the original waveform.

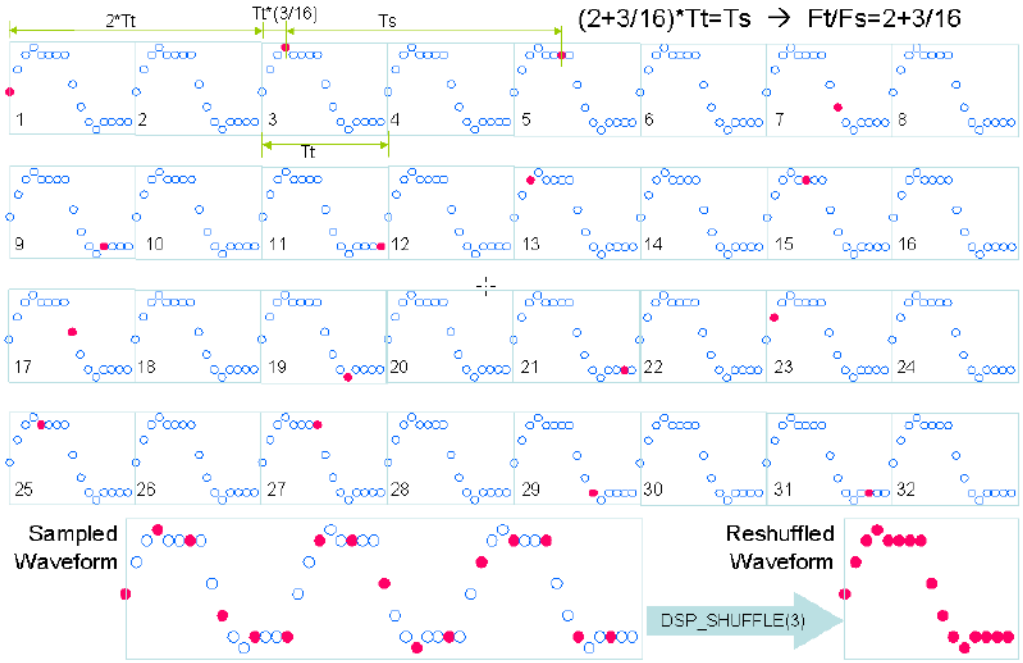


Figure 11: Under-sampling (2)

Figure 12 shows the case of M/N=K+Mx/N=2-1/16 so that Mx=-1. The sampled data directly replicates a single cycle of the original waveform, however it appears inside out.

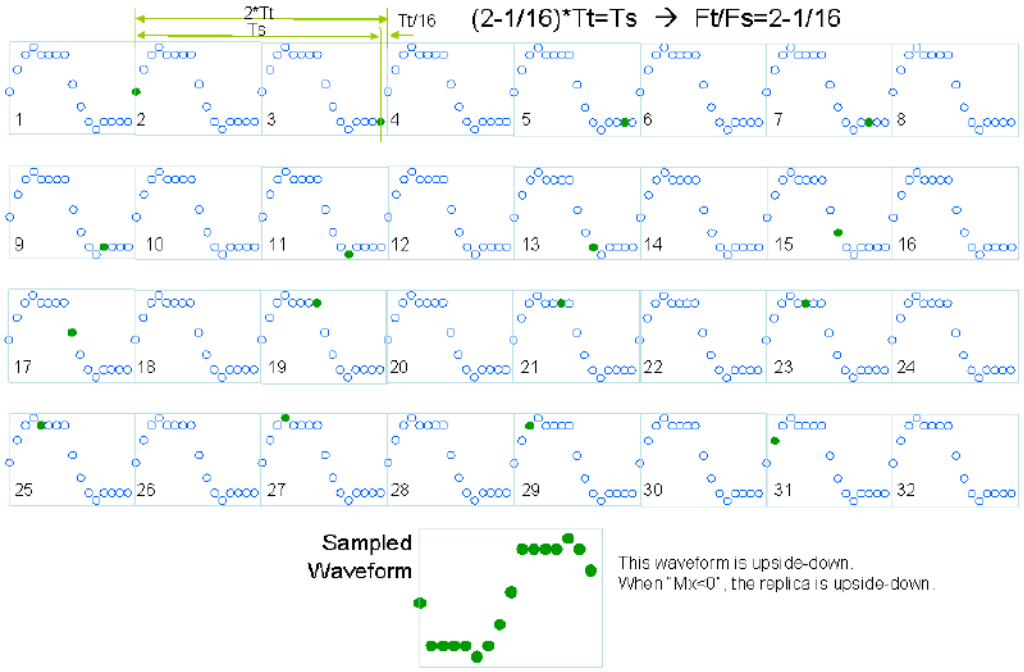


Figure 12: Under-sampling (3)

Figure 13 shows the case of M/N=K+Mx/N=2-3/16 so that Mx=-3. This is also the case of Mx<0. The sampled data captures 3 cycles of waveform so that DSP_SHUFFLE(3 cycles) replicates a single cycle of the original waveform. However, it appears inside out again.

As you already notice, when Mx is negative, the waveform is reconstructed inside out. It is no problem for the usual spectrum analysis. If you would feel uneasy with the waveform inside out, you may want to re-align the data array.

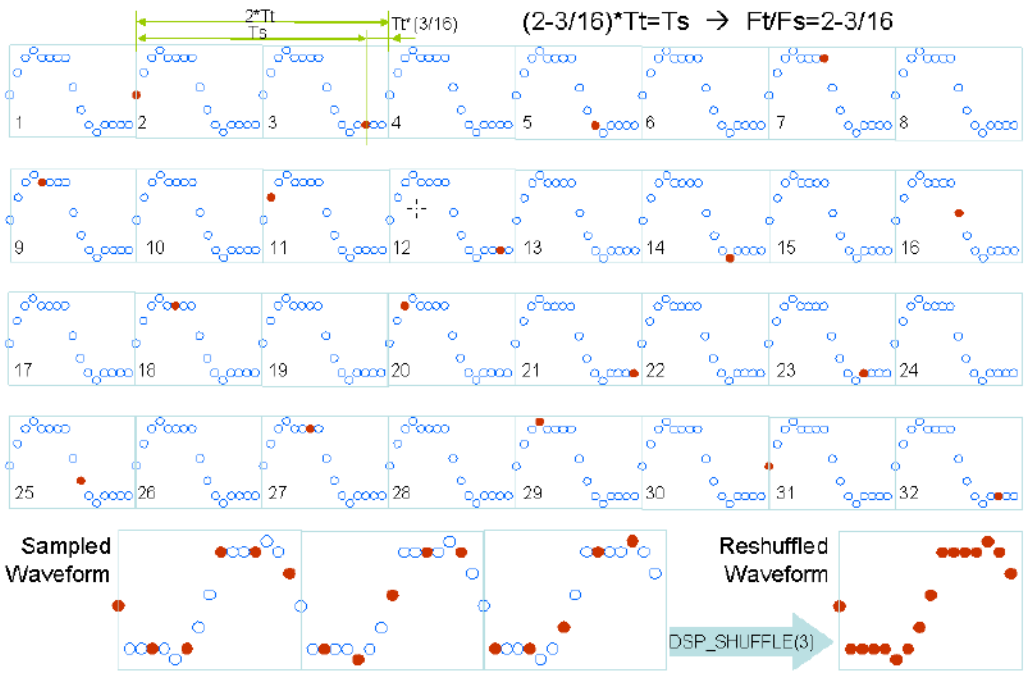


Figure 13: Under-sampling (4)

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